Solutions

Marking: **M1** a correct method, **A1** the correct answer, **B1** an independent mark.

Each answer shows the steps, then the **result**.

2.1

(a) `0xAF`; (b) `0xA5` AND `0x7E` = `0x24`; (c) `0x5A`

2.2

`(REG >> 8) & 0x7u`; `0x3A` AND `0x7` = **2**; `(0x3A5C & ~0x0700) | (6u << 8)` = `0x385C` OR `0x0600` = `0x3E5C`

2.3

the compiler sees nothing in the loop that changes the value, so it reads the register once and loops for ever on the old value; declare it `volatile uint32_t`, so every pass reads the hardware; a variable written by an interrupt routine and read in the main loop

2.4

65 536 ms = **65.5 s**; 2^{32} ms = **49.7 days**; $(500 - 65\,000) \bmod 65\,536$ = **1036 ms**, the true interval

3.1

`#define DIR (*(volatile uint32_t *)0x40020000u)`, with OUT at `0x40020004u` and IN at `0x40020008u`

```
DIR |= (1u << 5);

while (1) { if ((IN & (1u << 6)) == 0) OUT |= (1u << 5); else OUT &= ~(1u << 5); }
```

`OUT |=` is read–modify–write: if the interrupt toggles pin 7 between the read and the write, the main loop writes back the old pin 7; use the port's atomic set/reset register, or disable interrupts around the update

3.2

`r3` holds the address of `a[0]`, `0x2000_0100`; each word is 4 bytes, so `LSL #2` turns the index into a byte offset

`r0` = $3 + 5 + 7 + 9$ = **24**, `r1` = **4**

one pass = $2 + 1 + 1 + 1 + 3 = 8$ cycles, the last pass $8 - 3 + 1 = 6$

$2 + 3 \times 8 + 6$ = **32** cycles; $\dfrac{32}{84 \times 10^6}$ = **0.38 µs**

3.3

(a) $3 \times 4095 + 4095 = 16\,380$; below 65 535, so it fits

(b) at $y = 4092$: $\dfrac{3 \times 4092 + 4095}{4} = 4092.75$, and the shift drops the 0.75, so y stays at 4092; a steady error of 3 LSB from truncation

(c) $3 \times 65\,520 + 16 \times 4095 = 262\,080$; more than 65 535, so `uint32_t`

(d) float: $2000 \times 100 = 2 \times 10^5$ cycles/s = 0.24%; integer: 0.01%; both are tiny, so either works; ship the integer version for smaller code and the same result every run, or float if clarity matters more, with a reason

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