1. What is the binary number 10110 in decimal?

   _____

2. Simplify A + A · B.

   ☐ A · B

   ☐ A + B

   ☐ 1

   ☐ A

3. A 4-to-1 MUX with select S1S0 = 10 outputs –

   ☐ D1

   ☐ D2: the select code read as a binary number

   ☐ The OR of all inputs

   ☐ Depends on the data values

4. An SR latch has Q = 1. S and R are both low. What is Q?

   ☐ Unpredictable

   ☐ It oscillates

   ☐ 0 – inputs low clear it

   ☐ 1 – the latch holds its state

5. A Moore machine's outputs change –

   ☐ Only after the clock, from state alone

   ☐ Mid-cycle with the inputs

   ☐ Never

   ☐ Twice per cycle

6. In a register with load-enable low, the stored bits follow the data inputs at each clock edge.

   ☐ True ☐ False

7. Any Verilog that simulates correctly can be turned into gates.

   ☐ True ☐ False

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9. A K-map group of four cells keeps which variables?

   ☐ All variables of the function

   ☐ The variables that change inside the group

   ☐ Depends on the Gray-code order

   ☐ Only the variables constant across the whole group

10. How many output lines does a decoder with 3 inputs have?

    _____

1. **22**

   $16 + 4 + 2 = 22$: add the weights under the 1s.

2. **A**

   Absorption: whenever $A \cdot B$ is 1, A is already 1, so the term adds nothing. Check the four rows of A, B to confirm.

3. **D2: the select code read as a binary number**

   The select code names its data input: $10_2 = 2$, so D_2 passes. The MUX is a switch and does not look at the data.

4. **1 − the latch holds its state**

   With both inputs low the cross-coupled gates keep each other in place, which is exactly the memory. Only S = R = 1 is forbidden.

5. **Only after the clock, from state alone**

   Moore outputs are decoded from the state only, so they settle one clock after the input. Mealy adds the input for a same-cycle response, at the cost of possible glitches.

6. **False**

   With load-enable low each flip-flop is fed its own output, so it keeps its value. Only an enabled edge loads new data.

7. **False**

   Simulation accepts constructs with no hardware meaning, such as delays and ‘$display‘. Only the synthesizable subset becomes gates.

8. **63**

   $3 \times 16 + 15 = 63$. In binary it is 0011 1111.

9. **Only the variables constant across the whole group**

   A variable that takes both values inside the group cannot tell the cells apart, so it drops out. The odd-row group keeps only C because A and B both change inside it.

10. **8**

    $2^3 = 8$ outputs, one per minterm, with exactly one high at a time.

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