

5.5 Small-signal amplifiers

Name: _____ Class: _____ Date: _____

Total: **22 marks****KEY WORDS** small-signal • bias point • voltage gain

Objective

Linearise transistor stages about their bias points, compute g_m/r_π , evaluate the standard amplifier topologies' gains and resistances, and predict swing limits – every small-signal answer checked at a limiting case.

1 Key knowledge and worked examples

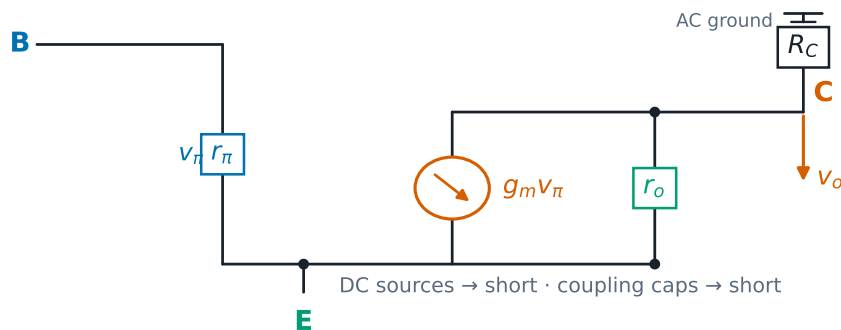
■ The small-signal parameters

At a **bias point** _____, the **small-signal** _____ model linearises the device:

- BJT: $g_m = I_C/V_T$ ($V_T = 26mV$), $r_\pi = \beta/g_m$, output $r_o = V_A/I_C$.
- MOSFET: $g_m = 2I_D/(V_{GS} - V_t)$ (square-law), r_o likewise.

In the signal circuit: DC sources $\rightarrow$ shorts; coupling capacitors $\rightarrow$ shorts (at signal frequency); the DC current source $\rightarrow$ open.

The hybrid- π model of the common-emitter stage



The hybrid- π model: one linear circuit for every small-signal question.

■ Worked example: the common-emitter stage

Bias $I_C = 1.1mA$, $\beta = 100$, $R_C = 2.2k\Omega$, R_E bypassed, $r_o \gg R_C$:

- $g_m = 1.1m/26m = 42.3mS$; $r_\pi = 100/42.3m = 2.36k\Omega$.
- Gain $A_v = -g_m \cdot R_C = -93$ (inverting).
- Input resistance $R_{in} = R_B \parallel r_\pi$; output resistance $\approx R_C$.

Limiting check: unbypass R_E and the gain becomes $-R_C/R_E = -2.2$ – the emitter degeneration trades gain for linearity and input resistance, exactly the factor predicted. Swing limit: the collector sits at $9.58V$ ($V_{CE} = 8.48V$), so it can rise $2.42V$ to the $12V$ rail before cut-off clips the positive swing and fall about $8.3V$ before saturation clips the negative – the symmetric swing is roughly $\pm 2.4V$.

■ The topology table

- **Common emitter** : high gain, inverted, moderate R_{in} .
- **Common collector / source follower** : gain $\approx g_m R_E / (1 + g_m R_E) < 1$, very high R_{in} , low R_{out} – a buffer.
- **Common base / gate**: gain $\approx +g_m R_C$, low R_{in} , non-inverting – the cascode's top half.

The cascode rule: a stage loads the previous one by its R_{in} in parallel with the bias network – gain multiplies only after that division.

2 Practice

2.1 A BJT at $I_C = 2mA$ ($\beta = 150$): compute g_m and r_π . [2]

2.2 A CE stage with $g_m = 40mS$, $R_C = 1.5k\Omega$, $R_E = 500\Omega$ unbypassed: compute the gain and verify against $-R_C/R_E$. [2]

2.3 A source follower with $g_m = 2mS$, $R_S = 500\Omega$: compute the gain and the output resistance $\approx 1/g_m$. [3]

3 Exam-style questions

3.1 A CE amplifier: $I_C = 1\text{mA}$, $\beta = 120$, $R_C = 4\text{k}\Omega$, $R_E = 400\Omega$ (bypassed by a large capacitor), $R_1 = 120\text{k}\Omega$, $R_2 = 30\text{k}\Omega$ (divider), and a load $R_L = 10\text{k}\Omega$ coupled through a capacitor. r_o is negligible.

Draw (describe) the small-signal circuit; compute g_m , r_π , the input resistance, and the loaded voltage gain $A_v = -g_m(R_C \parallel R_L)$. Then compute the unloaded gain and the loading loss in dB. State the swing limit set by the bias V_{CE} . [8]

3.2 A two-stage amplifier: a source follower ($g_{m1} = 2\text{mS}$, $R_S = 1\text{k}\Omega$) buffering a CE stage ($g_{m2} = 50\text{mS}$, $R_C = 2\text{k}\Omega$, $R_L = 3\text{k}\Omega$ AC-coupled).

Compute the follower's gain, the CE stage's loaded gain, and the overall voltage gain in dB. Then explain why inserting the follower between a high-impedance source and the CE stage improves the total gain (state what the gain would be without the buffer if the source had $100\text{ k}\Omega$ output resistance, given the CE input resistance is $2\text{ k}\Omega$). [7]
