

5.4 MOSFET biasing

Name: _____ Class: _____ Date: _____

Total: 24 marks

KEY WORDS MOSFET

- square-law model
- threshold
- saturation region

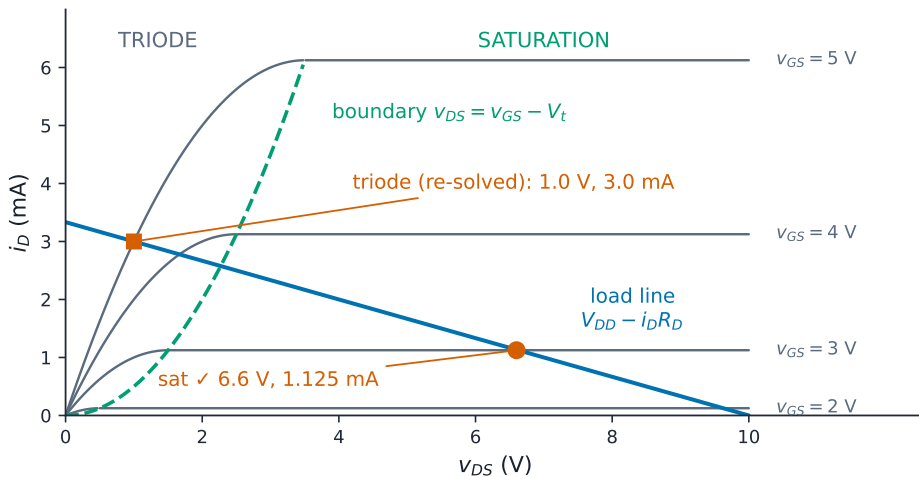
Objective

Bias MOSFETs with the square-law model, verify the saturation-region assumption, and design gate dividers – noting the MOSFET gate draws no DC current.

1 Key knowledge and worked examples

■ The square law in saturation

In **saturation** (the MOSFET's amplifier region), the **square-law model** gives $i_D = \frac{1}{2}k_n(W/L)(v_{GS} - V_t)^2$. Regions by comparison: cut-off ($v_{GS} < V_t$), triode ($v_{DS} < v_{GS} - V_t$), saturation ($v_{DS} \geq v_{GS} - V_t$). The gate is insulated – zero DC gate current, so gate dividers divide exactly.



The boundary parabola is the region test; both worked examples sit on this map.

■ Worked example: assume, solve, check

$V_{DD} = 10V$, $V_G = 3V$, $R_D = 3k\Omega$, $\frac{1}{2}k_n(W/L) = 0.5mA/V^2$, $V_t = 1.5V$.

- Assume saturation: $I_D = 0.5m \times (3 - 1.5)^2 = 1.125mA$.
- $V_{DS} = 10 - 1.125m \times 3k = 6.63V$.
- Check: $V_{DS} = 6.63 \geq V_G - V_t = 1.5$ ✓ saturation stands.
- Power: $P_D = V_{DS} \times I_D = 7.5mW$.

Had the check failed – e.g. the gate at 5V: saturation would want $V_{DS} = 10 - 6.1m \times 3k = -8.4V$, impossible – the triode equation $i_D = \frac{1}{2}k(W/L)[2(v_{GS} - V_t)v_{DS} - v_{DS}^2]$ takes over with the load line and gives $v_{DS} = 1.0V$, $i_D = 3.0mA$ (the figure's second point).

■ The CMOS inverter bias

An n-MOS pull-down and p-MOS pull-up make the logic inverter: input high turns the n-channel hard on (output low); input low turns the p-channel on (output high). At the switching threshold both conduct briefly – the **cross-coupled** gain region that gives the sharp transfer characteristic, and the seat of the short-circuit current a slow input edge suffers.

2 Practice

2.1 $\frac{1}{2}k(W/L) = 0.2mA/V^2$, $V_t = 1V$, $V_{GS} = 3V$: compute I_D (saturation). [2]

2.2 Same device with $V_{DD} = 12V$, $R_D = 4k\Omega$, $V_G = 5V$: compute V_{DS} and check the region. [4]

2.3 A MOSFET gate divider: $V_{DD} = 9V$, $R_1 = 100k\Omega$, $R_2 = 50k\Omega$. Give V_G exactly (no gate current) and note why the divider values can be far larger than a BJT's. [3]

3 Exam-style questions

3.1 Design a saturation-biased stage: $V_{DD} = 12V$, $\frac{1}{2}k(W/L) = 0.4 \text{ mA/V}^2$, $V_t = 2 \text{ V}$; targets $I_D = 2 \text{ mA}$ with $V_{DS} = 5 \text{ V}$.

Compute the required V_{GS} (from the square law inverted), the gate voltage V_G , and R_D (from the V_{DS} target). Verify saturation. Then compute the transconductance $g_m = 2 \cdot \frac{1}{2}k(W/L)(V_{GS} - V_t)$ at the bias point and the stage's small-signal gain $-g_m R_D$. [8]

3.2 A source-follower: $V_{DD} = 10V$, $\frac{1}{2}k(W/L) = 0.5 \text{ mA/V}^2$, $V_t = 1V$, $R_S = 1k\Omega$, gate at $V_G = 4V$ (stiff divider, no gate current).

Solve for I_D (square law + the source resistor: $V_{GS} = 4 - I_D \cdot 1k$) by solving the quadratic or iterating; compute V_S , V_{DS} , verify saturation, and state the follower's small-signal gain $g_m R_S / (1 + g_m R_S)$ at this bias. [7]
