5.3 BJT biasing

Name: _____ Class: _____ Date: _____ **Total: 24 marks**

KEY WORDS bipolar junction transistor • active region • voltage divider bias

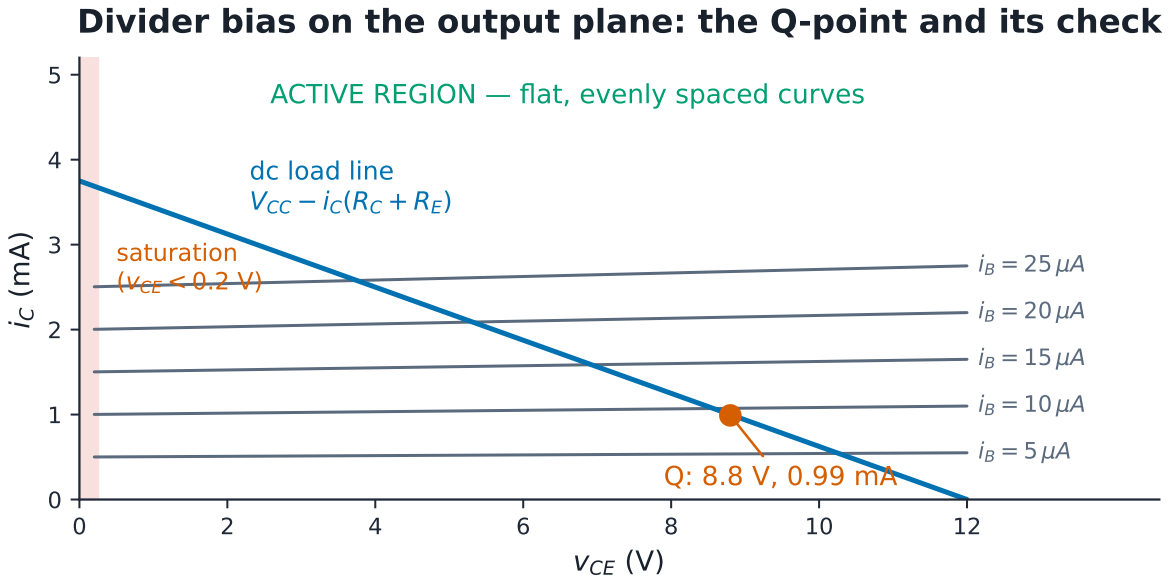
Objective

Design voltage-divider BJT bias points, verify the active region, and quantify bias stability against β spread – every bias checked against the region test.

1 Key knowledge and worked examples

■ The BJT's one rule of amplification

In the **active region** , $I_C = \beta \cdot I_B$ with $V_{BE} \approx 0.7V$; cut-off is $I_B = 0$; saturation is $V_{CE} \approx 0.2V$. The design task: put the bias point in the active region, centred so signal swings do not clip.



The 12 V dc load line ($RC + RE = 3.2\ k\Omega$) with the divider-bias Q-point at 0.99 mA, 8.8 V.

■ **Worked example: the divider bias, checked twice**

$V_{CC} = 12V$, $R_1 = 68k\Omega$, $R_2 = 12k\Omega$, $R_C = 2.2k\Omega$, $R_E = 1k\Omega$, $\beta = 100$. Thevenin: $V_B = 12 \times 12/80 = 1.8V$, $R_B = 68k \parallel 12k = 10.2k\Omega$. Then $V_E = 1.1V$, $I_C \approx 1.1mA$, $V_C = 9.58V$, $V_{CE} = 8.48V$.

Check 1 (region): $V_{CE} = 8.48 > 0.2$ – active ✓. Check 2 (stability): the exact $I_E = (V_B - 0.7)/(R_E + R_B/(\beta + 1))$ gives 1.00 mA at $\beta = 100$ and 1.05 mA at $\beta = 200$ – a 5% shift for a β doubling, because R_E dominates the denominator. That is the divider bias's whole purpose.

■ **Design rules of thumb**

- Make the divider stiff: $R_1 \parallel R_2 \leq \ \beta_{min} \cdot R_E/10$ – the base draws little.
- Put V_E near 0.1–0.2V_{CC} (thermal stability via R_E).
- Aim $V_{CE} \approx V_{CC}/2$ at the bias point for maximum symmetric swing.

2 Practice

2.1 $V_{CC} = 10V$, $R_1 = R_2 = 20k\Omega$, $R_E = 1k\Omega$, $R_C = 2k\Omega$, $\beta = 100$: find V_B, I_C, V_{CE} and name the region. [4]

2.2 Recompute 2.1's I_C with $\beta = 50$ using the exact formula $I_E = (V_B - 0.7)/(R_E + R_B/(\beta + 1))$; give the percentage shift. [3]

2.3 A fixed-bias circuit (R_B from V_CC to base, no R_E): state why its I_C tracks β directly and so is unstable. [2]

3 Exam-style questions

3.1 Design a divider bias for $V_{CC} = 12V$, $\beta \approx 150 (range 100–300)$, targeting $I_C = 2mA$ and $V_{CE} \approx 6V$, with R_E chosen for stability and the divider ten times stiffer than the base load.

Choose R_E (from a $V_E \approx 1.5V$ target), R_C (from the V_{CE} target), and R_1, R_2 (from V_B and the stiffness rule); compute the bias point at $\beta = 100$ and $\beta = 300$ and verify active-region operation and the I_C shift. [8]

3.2 An emitter-bias circuit has $V_{CC} = 15V$, $R_C = 3k\Omega$, $R_E = 2k\Omega$, and a base held at $V_B = 4V$ (a stiff divider; ignore its loading).

Compute I_C, V_{CE}, and the power in R_C and the transistor. Then state the maximum R_C before saturation with everything else fixed, and verify by computing V_{CE} at that R_C. [7]