3.4 Latches and flip-flops

Name: _____ Class: _____ Date: _____ **Total: 21 marks**

KEY WORDS latch • flip-flop • clock edge • toggle • excitation table

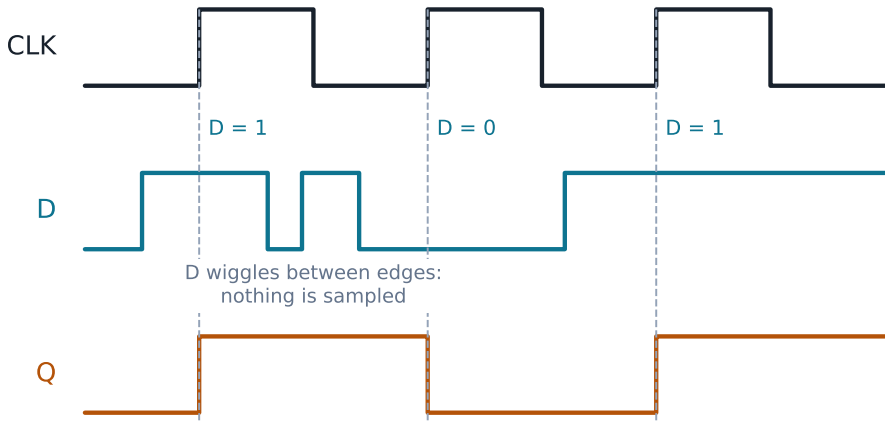
Objective

Trace latches and flip-flops on timing diagrams, use excitation tables to plan transitions, and distinguish level-sensitive from edge-triggered behaviour – every trace checked against the component's defining rule.

1 Key knowledge and worked examples

■ Latch: level-sensitive

A **latch** follows its input while enabled. The D latch with $EN = 1$ copies D to Q continuously ("transparent"); with $EN = 0$ it freezes Q. The SR latch (two cross-coupled NORs) sets on S, resets on R, holds on 00 – and `S = R = 1` is the forbidden combination.



■ Flip-flop: edge-triggered

A **flip-flop** samples only at the **clock edge** . The D flip-flop's one rule: `Q(next edge) = D(before that edge)`. Between edges, D may change freely – nothing happens. The J-K extends SR with $J = K = 1$ meaning **toggle** .

Worked example. D flip-flop, D sequence `1, 0, 1` at three rising edges: Q reads `1, 0, 1` after each edge. If D wiggles $1 \to 0 \to 1$ between edges 1 and 2, Q still holds its last sampled value – the timing diagram shows Q changing ONLY at edge instants. That is the entire difference from the latch.

■ Excitation tables: design in reverse

Given a desired $Q \to Q^+$ transition, the **excitation table** lists the inputs required:

$Q \to Q^+$	D	J K	T
$0 \to 0$	0	$0\ \times$	0
$0 \to 1$	1	$1\ \times$	1
$1 \to 0$	0	$\times\ 1$	1
$1 \to 1$	1	$\times\ 0$	0

(the $\times$ entries are free choices – J-K design exploits them to minimise logic). $D = Q^+$ always; $T = 1$ exactly when the state changes.

2 Practice

2.1 A D latch (EN = 1) sees D change $0 \to 1 \to 0$ over 60 ns. What does Q do, and when? [2]

2.2 A D flip-flop clocks on rising edges at t = 10, 20, 30 ns; D is 0 at 10, 1 at 20, 1 at 30. Give Q after each edge. [3]

2.3 From the excitation table: for $1 \to 0$ give the D input, the J-K inputs (one valid pair), and T. [3]

3 Exam-style questions

3.1 A J-K flip-flop starts at Q = 0 and receives (J, K) = (1, 0), (1, 1), (0, 1), (1, 1) at four successive falling edges.

Give Q after each edge with one line of reasoning each. Then state what makes (1, 1) different here from the SR latch's forbidden state. [6]

3.2 A D flip-flop's clock rises at 0, 10, 20, 30, 40 ns. D(t) is 1 for $0 \leq t < 15$, then 0 for $15 \leq t < 25$, then 1 for $t \geq 25$.

Draw (describe) Q(t) piecewise, giving its value after each edge. State the value sampled at t = 20 and why the D-change at t = 25 does not appear until t = 30. Explain why the same D stream into a D latch with EN high from t = 20 would differ at once. [7]