12.7 Signal-processing project

Name: _____ Class: _____ Date: _____ **Total: 25 marks**

KEY WORDS processing gain • resolution

Objective

Turn a specification into a verified pipeline and report measured margins honestly.

1 Key knowledge and worked examples

■ The method

Specify first (tone detector: 1 Hz bins, under 1 s latency, detect at −10 dB SNR); verify each stage alone (filter → window → FFT → threshold); report spec, measured and margin per line.

■ Worked example: the spec bites back

1 Hz bins at $f_s = 1$ kHz needs $N \geq 1000$ – already 1.0 s against the "<1 s" line. $N = 1024$: 0.977 Hz ✓, 1.024 s ×; $N = 1000$: exactly on the line. The margin table records the trade ✓.

■ The feasibility number

Processing gain $10 \log_{10}(N/2)$: 27 dB at $N = 1024$ – a −10 dB SNR tone becomes +17 dB in the decision bin ✓ detectable before anything is built.

2 Practice

2.1 Compute the bin processing gain at $N = 256$. [3]

2.2 A spec demands 0.5 Hz bins at $f_s = 2$ kHz. Minimum record length? [3]

2.3 Why is "tuning the detector until the lab tone is found" a defect rather than a method? [3]

3 Exam-style questions

3.1 A tone detector must find a 440 Hz tone within ±2 Hz at $f_s = 4$ kHz, reporting within 0.5 s, at −6 dB SNR.

Size N (power of two) and check the latency line. Compute the bin number of 440 Hz and the quantisation error in Hz. State the processing gain and the decision-bin SNR. State one spec line this design misses (or exactly meets) and its margin. [9]

3.2 The project report of a rival team claims “meets all specs” with a 6-line table where two rows read “PASS” but show no measured value.

Give the three defects of this table against the honest method. Compute what the missing numbers would need to show for a 1 Hz-bin spec with $N = 900$ at $f_s = 1$ kHz. State the single change that turns the table honest. [7]