

5.7 Frequency response of amplifiers

Name: _____ Class: _____ Date: _____

Total: 20 marks

KEY WORDS coupling capacitor • Miller capacitance • dominant pole

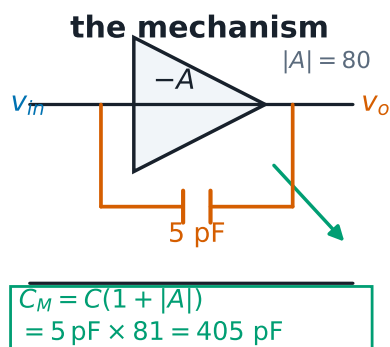
Objective

Locate low- and high-frequency corners from coupling capacitors and internal poles, apply the Miller multiplication, and compute bandwidth and gain-bandwidth limits – each corner checked against its own RC.

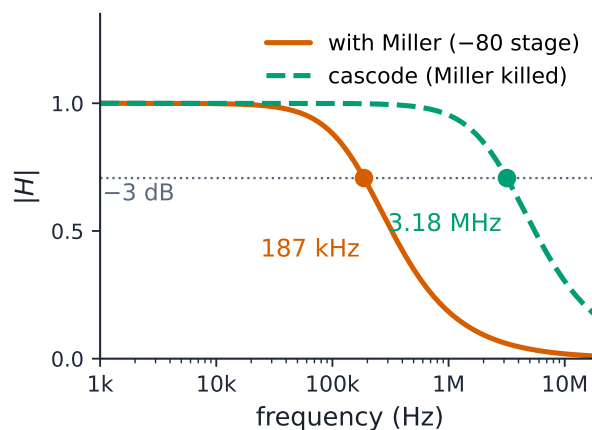
1 Key knowledge and worked examples

■ Two families of corner

Coupling capacitors (series, between stages) set the LOW corner $f_L = 1/(2\pi RC)$ per stage – the total low corner is the quadrature sum of stage corners. Internal capacitances set the HIGH corner via the **dominant pole** : $f_H \approx 1/(2\pi R_{eq} \cdot C_{eq})$ at the input node.



what it costs (and the cascode cure: 17×)



The Miller multiplication and the bandwidth it costs; the cascode reclaims 17×.

■ Worked example: Miller multiplication

A stage with gain -80 has $C_{gb} = 5pF$ base-to-collector. The input sees the **Miller capacitance** $C_M = C_{gb}(1 + |A_v|) = 5p \times 81 = 405pF$. With $R_{eq} = 2k\Omega$ and 20 pF stray: $f_H = 1/(2\pi \times 2000 \times 425p) = 187kHz$. The Miller effect explains why high-gain stages roll off first – and why the cascode (which holds the collector nearly still, killing the gain across C_{gb}) extends bandwidth for free.

■ Gain-bandwidth closure

For an op-amp stage, once f_H is known, the **gain-bandwidth product** closes the design: gain $\times$ bandwidth = constant. A discrete stage's own corners multiply the same way – two cascaded stages each -3 dB at a frequency give -6 dB total there, and the composite -3 dB point is lower than either.

2 Practice

2.1 A coupling capacitor 10 μF into a 15 $k\Omega$ input resistance: compute f_L . [2]

2.2 An input node with $R_{eq} = 4k\Omega$ and $C_{eq} = 50pF$: compute f_H . [2]

2.3 A stage of gain -50 has 4 pF across it: compute the Miller capacitance the input sees. [2]

3 Exam-style questions

3.1 A single-stage CE amplifier has: input coupling $2.2\ \mu\text{F}$ into a $20\ \text{k}\Omega$ total resistance; a bypass capacitor $47\ \mu\text{F}$ looking into $R_E \parallel (r_{\pi}/(\beta+1)) \approx 25\ \Omega$; and a high-frequency node of $R_{eq} = 1.5\ \text{k}\Omega$ with $C_{gb} = 4\ \text{pF}$ at stage gain -60 plus $25\ \text{pF}$ stray.

Compute each low corner (coupling, bypass) and the high corner (with Miller); state the amplifier's passband edges; and compute the bypass capacitor needed to push ITS corner a decade below the coupling corner. [7]

3.2 A two-stage amplifier has each stage at gain -40 with input $R_{eq} = 2\ \text{k}\Omega$, $C_{gb} = 5\ \text{pF}$, stray $20\ \text{pF}$.

Compute each stage's Miller capacitance and f_H ; compute the composite $-3\ \text{dB}$ high corner of the cascade (quadrature combination: $1/f_{\text{total}}^2 \approx 1/f_1^2 + 1/f_2^2$ for two identical stages – equivalently $f_{\text{total}} = f_H \cdot \sqrt{2^{\{1/2\}} - 1}^{\{1/2\}} = 0.644\ f_H$); and state the gain-bandwidth product of one stage. Verify the composite against the per-stage corner. [7]

Solutions

2.1

- $f_L = 1/(2\pi \times 15k \times 10\mu) = 1.06Hz$.

2.2

- $f_H = 1/(2\pi \times 4k \times 50p) = 796kHz$.

2.3

- $C_M = 4p \times (1 + 50) = 204pF$.

3.1

- Coupling corner: $1/(2\pi \times 20k \times 2.2\mu) = 3.6Hz$.
- Bypass corner: $1/(2\pi \times 25 \times 47\mu) = 135Hz$.
- Miller: $4p \times 61 = 244pF$ (+25 pF = 269 pF); $f_H = 1/(2\pi \times 1.5k \times 269p) = 394kHz$.
- Passband: approximately 135 Hz (the bypass corner dominates the low end) to 394 kHz.
- Bypass a decade below 3.6 Hz needs $f = 0.36Hz$: $C = 1/(2\pi \times 25 \times 0.36) = 17.7mF$ – impractically large; that is why the bypass capacitor sets the real low corner in practice.

3.2

- Per stage: $C_M = 5p \times 41 = 205pF$ (+20 pF = 225 pF); $f_{-H} = 1/(2\pi \times 2k \times 225p) = 354 \text{ kHz}$.
- Composite (two identical stages): $f_{-3dB} = f_{-H} \times \sqrt{2^{1/2} - 1} = 354k \times 0.6436 = 228 \text{ kHz}$.
- GBW per stage: $|A| \times f_H = 40 \times 354kHz = 14.2MHz$.
- Verify: at 228 kHz each stage is $1/\sqrt{1 + (228/354)^2} = 1/\sqrt{1.414} = 0.841$ (−1.5 dB), two give −3 dB exactly ✓ – the composite math checks.