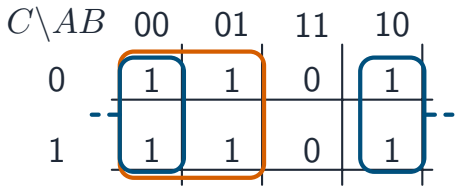
Exercise walk-through

3.4
Latches and flip-flops

University Electrical Engineering

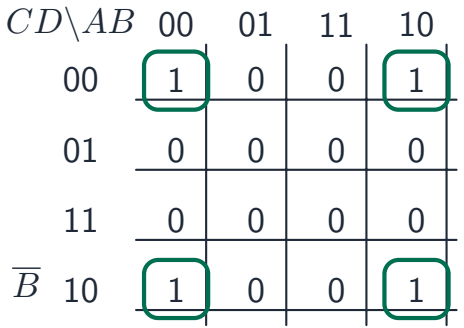
Loop the ones

three variables: the worked example



red loop of 4 (columns 00, 01): $A = 0$ throughout, so $\overline{A}$
blue loop of 4 wrapping round (columns 00, 10): $B = 0$, so $\overline{B}$
$Z = \overline{A} + \overline{B}$

four variables: a wrap-around loop

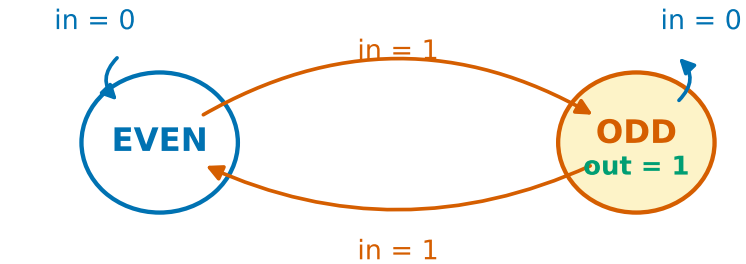


the four corners are one loop of 4: $B = 0$ and $D = 0$
in every corner, so the term is $\overline{B}\,\overline{D}$

> Bigger loops give simpler expressions

Two states, one flip-flop

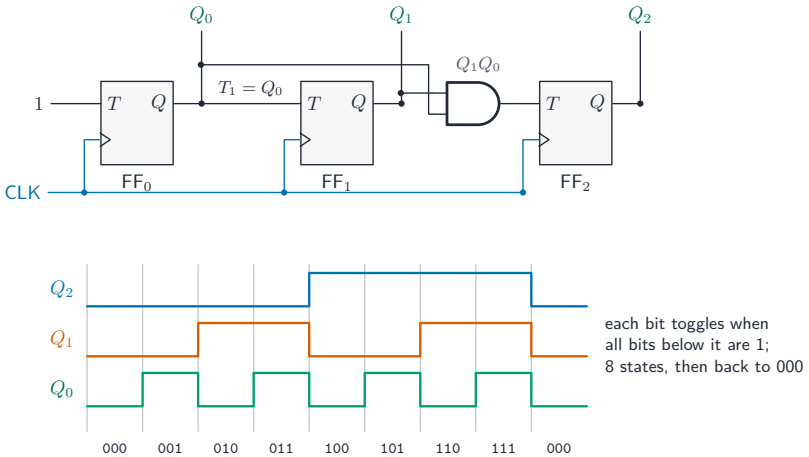
The parity detector: two states, one flip-flop



next-state logic: $Q^+ = Q \oplus in$ — the machine is a parity bit

EVEN and ODD swap on input 1, loop on 0; output = 1 in ODD. The next-state logic is Q xor in.

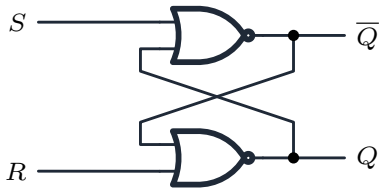
One clock, computed toggles



Toggle logic feeds a T flip-flop bank: T0 = 1, T1 = Q0, T2 = Q1 AND Q0 - trace 000, 001, 010, 011.

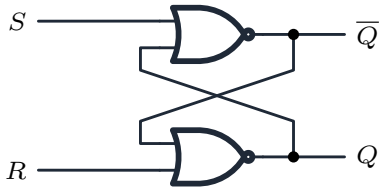
Exercise 2.1

2.1 The NOR SR latch shown starts with $Q = 0$. The inputs (S, R) go through the steps $(1,0)$, $(0,0)$, $(0,1)$, $(0,0)$, $(1,0)$. Give Q after each step. Which input pair must never be used, and why? [3]



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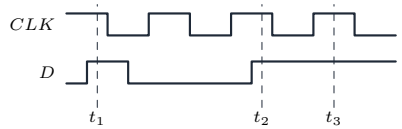


2.1

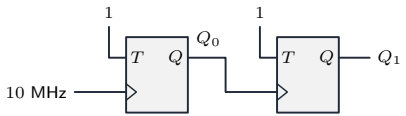
$Q = 1, 1, 0$ for the first three steps; then $0, 1$; $S = R = 1$ forces both outputs to 0, so Q and $\overline{Q}$ are not opposite, and the next state is unknown

Exercises 2.2·2.3

2.2 The clock CLK and the data D shown drive both a D latch (enabled by CLK) and a rising-edge D flip-flop. Both start at $Q = 0$. Find Q of each at the times t_1, t_2 and t_3. [3]

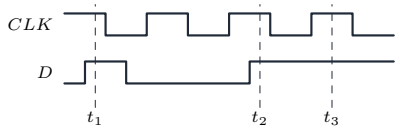


2.3 Two T flip-flops are chained as shown, with $T = 1$ on both. The first is clocked at 10 MHz. Find the frequency at Q_0 and at Q_1. [3]



Exercises 2.2·2.3

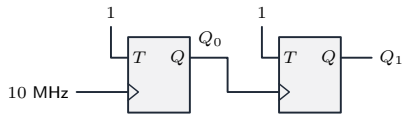
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2.2

latch: $Q = \mathbf{1}, \mathbf{1}, \mathbf{1}$; flip-flop: $Q = \mathbf{0}, \mathbf{0}, \mathbf{1}$; the latch follows D while $CLK = 1$, but the flip-flop only takes D at a rising edge, and D was 0 at the first three edges

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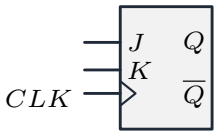
2.3

$Q^+ = T \oplus Q = \overline{Q}$: it toggles on every edge; Q_0: **5.0 MHz**; Q_1: **2.5 MHz**

exercises.lol exercises.com.cn

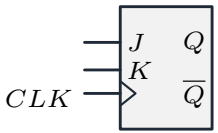
Exercise 2.4

2.4 Give J and K for a JK flip-flop that must go $0 \to 0$, $0 \to 1$, $1 \to 0$ and $1 \to 1$ (its excitation table). Use X for "either". Check one row with $Q^+ = J\overline{Q} + \overline{K}Q$. [3]



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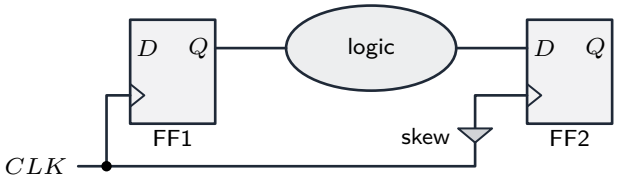
2.4

$0 \to 0$: $J = 0$, $K = X$; $0 \to 1$: $J = 1$, $K = X$; $1 \to 0$: $J = X$, $K = 1$; $1 \to 1$: $J = X$, $K = 0$; check $1 \to 0$: $Q = 1$, $K = 1$: $Q^+ = J \cdot 0 + 0 \cdot 1 = 0$

Exercise 3.1

3.1 Flip-flop FF1 drives FF2 through logic with a delay of 3.6 ns (longest path) and 0.2 ns (shortest path). $t_{cq} = 0.5$ ns (max) and 0.3 ns (min), $t_{su} = 0.4$ ns and $t_h = 0.3$ ns.

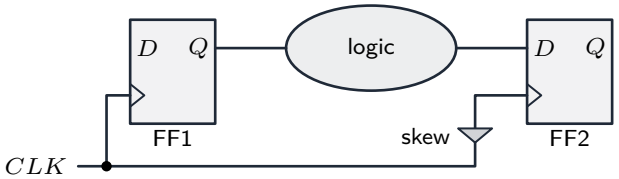
Find f_{max} and the hold margin. The clock now reaches FF2 0.4 ns late. Check hold again, and suggest a fix if it fails. [5]



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Find f_{max} and the hold margin. The clock now reaches FF2 0.4 ns late. Check hold again, and suggest a fix if it fails. [5]



3.1

$T_{min} = 0.5 + 3.6 + 0.4 = 4.5$ ns, $f_{max} =$ **222 MHz**

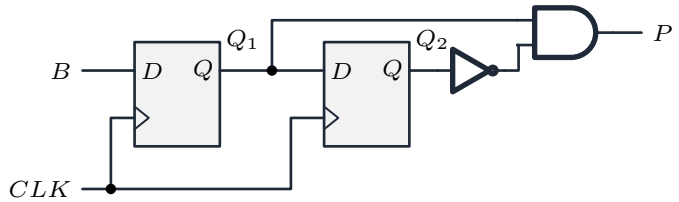
hold: $0.3 + 0.2 = 0.5 \geq 0.3$ ns, margin **0.2 ns**

late clock: FF2 needs $0.3 + 0.4 = 0.7$ ns, but the data changes after 0.5 ns: **hold fails**; add delay (buffers) of at least 0.2 ns in the short path

Exercise 3.2

3.2 The circuit shown samples a slow push-button signal B. At each rising edge $Q_1 \leftarrow B$ and $Q_2 \leftarrow Q_1$, and $P = Q_1 \cdot \overline{Q_2}$. All start at 0. B goes high just before edge 2 and stays high.

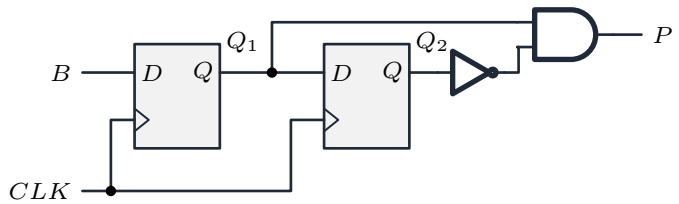
Give Q_1, Q_2 and P after edges 1 to 5. What does the circuit do, and what is it used for? [5]



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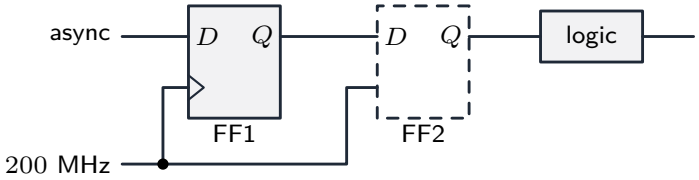
$Q_1 = 0, 1, 1, 1, 1$; $Q_2 = 0, 0, 1, 1, 1$; $P = 0, 1, 0, 0, 0$

P is high for exactly one clock period after B rises: a rising-edge detector; it lets a counter or a state machine count each press once, however long the button is held

Exercise 3.3 (a)

3.3 An asynchronous signal enters a 200 MHz clock domain. It changes about 10^6 times a second. The flip-flops have $\tau = 100$ ps, $T_0 = 20$ ps and $t_{su} = 0.4$ ns.

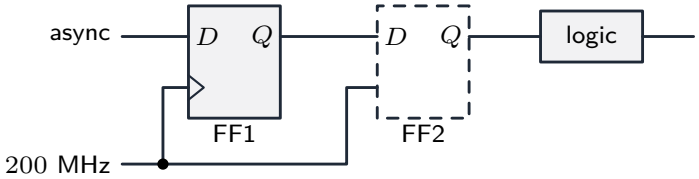
(a) With one flip-flop, logic of 3.0 ns follows before the next flip-flop. Find the settling time t_r and the MTBF. [3]



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(a) $t_r = 5.0 - 3.0 - 0.4 = \mathbf{1.6\ ns}$; $T_0 f_{clk} f_{data} = 20 \times 10^{-12} \times 2 \times 10^8 \times 10^6 = 4000\ \mathrm{s}^{-1}$, and $e^{16} = 8.9 \times 10^6$; MTBF $= \mathbf{2.2 \times 10^3\ s}$, about 37 minutes

Exercise 3.3 (b)

3.3 An asynchronous signal enters a 200 MHz clock domain. It changes about 10^6 times a second. The flip-flops have $\tau = 100$ ps, $T_0 = 20$ ps and $t_{su} = 0.4$ ns.

(b) A second flip-flop (dashed) is added, so FF1 has a whole period minus setup to settle. Find the new MTBF. [3]

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(b) A second flip-flop (dashed) is added, so FF1 has a whole period minus setup to settle. Find the new MTBF. [3]

(b) $t_r = 5.0 - 0.4 = 4.6$ ns; MTBF $= \dfrac{e^{46}}{4000} = \mathbf{2.4 \times 10^{16}}$ **s** $\approx 7.5 \times 10^8$ years

Exercise 3.3 (c)

3.3 An asynchronous signal enters a 200 MHz clock domain. It changes about 10^6 times a second. The flip-flops have $\tau = 100$ ps, $T_0 = 20$ ps and $t_{su} = 0.4$ ns.

(c) One million units will run for 10 years. Judge each design. [2]

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(c) one flip-flop fails every 37 minutes in every unit: not acceptable; two flip-flops: $7.5 \times 10^8 / 10^6 = 750$ years between failures across the whole fleet, far above 10 years, for one extra clock of delay: use two