Solutions

2.1

- $2^{13}/2^4 = 512$ lines: index 9 bits, offset 4 bits ✓.

2.2

- $1 + 0.05 \times 40 = 3$ cycles ✓.

2.3

- Temporal (reuse) and spatial (adjacency) ✓.

3.1

- $2^{11}/32 = 64$ lines: offset 5 bits, index 6 bits, tag $32 - 11 = 21$ bits ✓.
- $0x7CE = 0111\,1100\,1110_2$ (low 11 bits): offset $01110_2 = 14$; index $111110_2 = 62$ – line 62 of 64 ✓.
- Two hot blocks in one slot evict each other turn by turn – a conflict miss ✓.
- AMAT $= 1 + 0.04 \times 50 = 3$ cycles ✓.

3.2

- A (row-major): one miss per line – 4 ints per line – miss rate $1/4 = 25\%$ (compulsory only) ✓.
- B (column-major): successive elements sit $128 \times 4 = 512$ bytes apart – one per line, miss rate 100% ✓.
- AMATs: A $= 1 + 0.25 \times 40 = 11$ cycles; B $= 1 + 1.0 \times 40 = 41$ cycles – a 3.7× multiplier ✓.
- A bigger cache holds more lines but the stride still touches one int per line: bandwidth per line, not capacity, is the wall ✓.