

Exercise walk-through

6.5

Input/output

University Computer Science

Input/output: three ways to move a block

- 1 **Poll** Flag every 2 microseconds, poll 50 cycles at 250 ps: 160 polls per event, 8000 cycles of attention per word.
- 2 **Interrupt** The handler costs 200 cycles per word; receiving 1024 words one interrupt each: 204 800 cycles of overhead.
- 3 **DMA** One 500-cycle setup plus one 200-cycle completion for 1024 words: 0.68 cycles per word - 292 times less than per-word interrupts.

Three I/O paths

three ways to move one block

polling

core spins on status
160 polls per event
8000 cycles per word

interrupts

device signals ready
200-cycle handler
200 cycles per word

DMA

engine moves the block
one interrupt at the end
0.68 cycles per word

CPU attention per word: 8000 vs 200 vs 0.68 cycles - the same bytes, three bills

rule of thumb: poll what must be sampled, interrupt what arrives, DMA what streams

Polling burns the core; interrupts charge per event; **DMA** charges once per block.

Exercises 2.1-2.3

2.1 A device flags every 4 μs ; one poll is 12.5 ns. How many polls per event? [3]

2.2 Name the style for a keyboard. [3]

2.3 Name the style for a 2 GB/s disk stream. [3]

Exercises 2.1-2.3

2.1 A device flags every 4 μs ; one poll is 12.5 ns. How many polls per event? [3]

2.1

- $4\ \mu\text{s}/12.5\ \text{ns} = 320\ \text{polls}\ \checkmark$.
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2.2 Name the style for a keyboard. [3]

2.2

- Interrupts – rare human-paced events $\checkmark$.
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2.3 Name the style for a 2 GB/s disk stream. [3]

2.3

- DMA – streaming blocks $\checkmark$.

Exercise 3.1

3.1 A sensor must be sampled every $8\text{ }\mu\text{s}$; one poll costs 100 cycles at 250 ps; the interrupt handler costs 400 cycles.

Compute the polls per sample and the cycles of CPU attention per sample under continuous polling. Compute the attention per sample under interrupts (one event per sample). State which style fits and why, naming the criterion. [8]

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3.1

- Polls per sample: $8\text{ }\mu\text{s}/25\text{ ns} = 320$ (one poll = $100 \times 250\text{ ps} = 25\text{ ns}$) ✓.
- Polling attention: $320 \times 100 = 32\,000$ cycles per sample ✓.
- Interrupt attention: 400 cycles per sample – $80\times$ less ✓.
- Sampling at a fixed rate fits polling only if the loop is dedicated; with any other work, interrupts win – the criterion is whether the CPU has anything else to do ✓.

Exercise 3.2

3.2 A 2048-word block arrives; per-word interrupts cost 200 cycles each; DMA costs a 600-cycle setup plus a 200-cycle completion interrupt.

Compute the total CPU cycles both ways and the ratio. Compute the bytes per interrupt a design must average to keep DMA overhead under 1% of a 200-cycle-per-word alternative. State what still costs the CPU under DMA. [7]

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3.2

- Per-word interrupts: $2048 \times 200 = 409\,600$ cycles ✓.
- DMA: $600 + 200 = 800$ cycles; ratio $409\,600/800 = 512\times$ ✓.
- Under 1% of $200 \times n$ cycles with one 800-cycle DMA bill: $800 < 0.01 \times 200n \Rightarrow n > 400$ words per interrupt ✓.
- Under DMA the CPU still pays the setup, the completion handling, and cache-coherence care – the data path, not the data movement ✓.