1. The ISA is best described as –

   ☐ the contract between compiler and hardware

   ☐ the cache size

   ☐ the wires inside the ALU

   ☐ the clock speed

2. The single-cycle clock must wait for –

   ☐ the cache only

   ☐ the shortest instruction

   ☐ an average instruction

   ☐ the longest instruction path

3. Ten instructions on a five-stage pipeline take –

   ☐ 50 cycles

   ☐ 15 cycles

   ☐ 10 cycles

   ☐ 14 cycles

4. A 4 KiB direct-mapped cache with 16-byte lines has – index bits

   ☐ 8

   ☐ 12

   ☐ 4

   ☐ 20

5. DMA differs from interrupt-driven I/O because it –

   ☐ interrupts per word

   ☐ polls the device

   ☐ moves the block and interrupts once

   ☐ needs no memory

6. A program is 95% parallelizable. What is the largest possible speedup by Amdahl's law?

   _____

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_____

8. A multi-cycle machine runs 40% loads (5 cycles) and 60% R-type (4 cycles). What is the CPI?

   _____

9. 25% of instructions are branches, the predictor is right 80% of the time, and a miss costs 3 cycles. With base CPI 1, what is the CPI?

   _____

10. A 4-way set-associative cache holds 4 KiB in 16-byte lines. How many index bits does an address need?

    _____

1. **the contract between compiler and hardware**

   It states everything software may rely on and nothing about implementation.

2. **the longest instruction path**

   All work fits in one clock, so lw (IM+RF+ALU+DM+wiring = 900 ps) sets the cycle.

3. **14 cycles**

   n + k − 1 = 10 + 5 − 1 = 14: fill four, then one per cycle.

4. **8**

   256 lines need log2 256 = 8 index bits; offset 4, tag 20.

5. **moves the block and interrupts once**

   A DMA engine owns the transfer; the CPU pays one setup plus one completion.

6. **20**

   The ceiling is 1 / (1 - 0.95) = 1 / 0.05 = 20.

7. **536**

   PC + 4 = 516, plus 4 x 5 = 20, gives 536.

8. **4.4**

   0.4 x 5 + 0.6 x 4 = 2.0 + 2.4 = 4.4.

9. **1.15**

   0.25 x 0.2 x 3 = 0.15 extra, so CPI = 1.15.

10. **6**

    256 lines / 4 ways = 64 sets, and 2^6 = 64.

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