6. Computer Architecture

Starter Quiz ·

University Computer Science Name: _____ Score: _____

1. The ISA is best described as –

   ☐ the contract between compiler and hardware

   ☐ the cache size

   ☐ the wires inside the ALU

   ☐ the clock speed

2. The single-cycle clock must wait for –

   ☐ the cache only

   ☐ the shortest instruction

   ☐ an average instruction

   ☐ the longest instruction path

3. Ten instructions on a five-stage pipeline take –

   ☐ 50 cycles

   ☐ 15 cycles

   ☐ 10 cycles

   ☐ 14 cycles

4. A 4 KiB direct-mapped cache with 16-byte lines has – index bits

   ☐ 8

   ☐ 12

   ☐ 4

   ☐ 20

5. DMA differs from interrupt-driven I/O because it –

   ☐ interrupts per word

   ☐ polls the device

   ☐ moves the block and interrupts once

   ☐ needs no memory

6. With f = 0.9, the speedup ceiling is –

   ☐ unbounded

   ☐ 10 times

- ☐ 0.9 times
- ☐ 9 times

7. A 16-bit signed immediate can hold –
   - ☐ 65 535
   - ☐ 32 767
   - ☐ any int
   - ☐ 40 000
8. With IM 200, RF 100, ALU 200, DM 250, wiring 150 ps, the lw cycle is –
   - ☐ 600 ps
   - ☐ 1050 ps
   - ☐ 900 ps
   - ☐ 750 ps
9. 1000 instructions, 25% loads, half load-use: total cycles –
   - ☐ 1029
   - ☐ 1129
   - ☐ 1000
   - ☐ 1250
10. Hit 1 cycle, miss ratio 2%, penalty 100: AMAT is –
    - ☐ 3 cycles
    - ☐ 101 cycles
    - ☐ 1.02 cycles
    - ☐ 2 cycles

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Answers ·

University Computer Science

1. **the contract between compiler and hardware**

   It states everything software may rely on and nothing about implementation.

2. **the longest instruction path**

   All work fits in one clock, so lw (IM+RF+ALU+DM+wiring = 900 ps) sets the cycle.

3. **14 cycles**

   n + k − 1 = 10 + 5 − 1 = 14: fill four, then one per cycle.

4. **8**

   256 lines need log2 256 = 8 index bits; offset 4, tag 20.

5. **moves the block and interrupts once**

   A DMA engine owns the transfer; the CPU pays one setup plus one completion.

6. **10 times**

   As p grows without bound, speedup tends to $1/(1 - f) = 10$.

7. **32 767**

   The range is −32 768 to 32 767; 40 000 needs two instructions.

8. **900 ps**

   200+100+200+250+150 = 900 ps – the slowest citizen.

9. **1129**

   1000 + 125 stalls + 4 fill = 1129, CPI 1.129.

10. **3 cycles**

    AMAT = $1 + 0.02 \times 100 = 3$ cycles; misses, not hits, set the sensitivity.