Computer Architecture

University Computer Science · Vocabulary in context

Word	Example
computer architecture	**Computer architecture** studies how the parts of a computer work together.
instruction set architecture	The **instruction set architecture** lists every instruction the CPU understands. CPU
RISC /rɪsk/	Most phones use a **RISC** processor, which has a small set of simple instructions.
load-store	In a **load-store** design, only load and store instructions use memory.
byte-addressable	In **byte-addressable** memory, every byte has its own address.
datapath	The **datapath** moves and changes data inside the CPU. CPU
control /kənˈtrəʊl/	The **control** unit tells each part of the CPU what to do. CPU
ALU /ˌeɪ el ˈjuː/	The **ALU** does the sums.
pipelining /ˈpaɪplaɪnɪŋ/	**Pipelining** works like a factory line: several instructions are in progress at once.
retires	An instruction **retires** when its result is final.
CPI	A **CPI** of 2 means each instruction takes two clock cycles on average. 2

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read-after-write hazard	A **read-after-write hazard** happens when an instruction needs a value that is not ready yet.
forwarding	**Forwarding** sends a result straight to the next instruction that needs it.
memory hierarchy	The **memory hierarchy** goes from small, fast cache to large, slow disk. ` `
locality	Using array items that sit next to each other shows good **locality**.
direct-mapped cache	In a **direct-mapped cache**, each memory block can go in only one slot.
tag /tæg/	The **tag** shows which memory block is in a cache slot.
index /ˈɪndeks/	Use **index** 3 to read the third item in the array. 3
block offset	The **block offset** picks one byte inside the block.
average memory access time	**Average memory access time** combines hit time, miss rate and miss penalty. ` `
evicts	A new block **evicts** the old one from the cache.
programmed I/O	In **programmed I/O**, the CPU keeps checking whether the device is ready. CPU
interrupt-driven I/O	With **interrupt-driven I/O**, the device tells the CPU when it is ready. CPU

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DMA	**DMA** moves data to memory without the CPU doing each step. CPU
instruction-level parallelism	**Instruction-level parallelism** runs several instructions at once in one core.
SMT	With **SMT**, one core runs two threads at the same time.
R-type	An **R-type** instruction uses only registers, such as add. add
I-type	An **I-type** instruction includes a number, such as addi. addi

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