UNIVERSITY COMPUTER SCIENCE • EXERCISE SHEET

7.4 Virtual memory

Name: _____ Class: _____ Date: _____ **Total: 24 marks**

KEY WORDS page table • TLB

Objective

Translate addresses through the page table and price the faults.

1 Key knowledge and worked examples

■ **The machine**

16-bit virtual, 256-byte pages: 256 pages; 12-bit physical: 16 frames ✓. $0x0204$ = offset 4, VPN 2 → frame 5 → physical $0x0504$; $0x0210$ hits the TLB at $0x0510$ ✓.

■ **Worked example: the fault's price**

TLB hit 1 ns, walk 10 ns, fault 5 ms; a fault per million accesses amortises to 5 ns per access ✓.

2 Practice

2.1 20-bit virtual addresses with 1 KiB pages: how many virtual pages, and how many VPN bits? [3]

2.2 VPN 7 maps to frame 3. Translate $0x0705$ (256-byte pages). [3]

2.3 Distinguish an invalid access from a page fault in one line. [3]

3 Exam-style questions

3.1 A machine has 24-bit virtual addresses, 2 KiB pages, and 1 MiB of physical memory.

Compute the page count, the VPN bits, the frame count and the frame bits, and the page-table entry count. Translate virtual $0x123456$ (offset, VPN). Compute the page-table size in bits if each entry holds frame bits + valid + dirty + reference. [8]

3.2 A process's accesses hit the TLB 98% of the time; a miss walks the table in 20 ns; 1% of walks fault, each costing 4 ms.

Compute the average access time (TLB hit 1 ns). Recompute with faults at 0.1% of walks. State which term dominates each answer and the one-line design lesson. [7]