UNIVERSITY COMPUTER SCIENCE • EXERCISE SHEET

6.5 Input/output

Name: _____ Class: _____ Date: _____ **Total: 24 marks**

KEY WORDS DMA • programmed I/O I/O

Objective

Price the three I/O styles in CPU cycles per word and choose by the shape of the traffic.

1 Key knowledge and worked examples

■ The three bills

Polling: 160 polls per 2 µs event at 12.5 ns a poll – 8 000 cycles of attention per word ✓. Interrupts: 200-cycle handler per word ✓. DMA: $500 + 200$ cycles per 1024-word block – 0.68 cycles per word ✓.

■ Worked example: the ratio

Per-word interrupts over DMA: $204\,800/700 \approx 292\times$ – the same bytes, three bills ✓.

2 Practice

2.1 A device flags every 4 µs; one poll is 12.5 ns. How many polls per event? [3]

2.2 Name the style for a keyboard. [3]

2.3 Name the style for a 2 GB/s disk stream. [3]

3 Exam-style questions

3.1 A sensor must be sampled every 8 µs; one poll costs 100 cycles at 250 ps; the interrupt handler costs 400 cycles.

Compute the polls per sample and the cycles of CPU attention per sample under continuous polling. Compute the attention per sample under interrupts (one event per sample). State which style fits and why, naming the criterion. [8]

3.2 A 2048-word block arrives; per-word interrupts cost 200 cycles each; DMA costs a 600-cycle setup plus a 200-cycle completion interrupt.

Compute the total CPU cycles both ways and the ratio. Compute the bytes per interrupt a design must average to keep DMA overhead under 1% of a 200-cycle-per-word alternative. State what still costs the CPU under DMA. [7]

Solutions

2.1

- $4\,\mu s / 12.5\,ns = 320$ polls ✓.

2.2

- Interrupts – rare human-paced events ✓.

2.3

- DMA – streaming blocks ✓.

3.1

- Polls per sample: $8\,\mu s / 25\,ns = 320$ (one poll $= 100 \times 250$ ps $= 25$ ns) ✓.
- Polling attention: $320 \times 100 = 32\,000$ cycles per sample ✓.
- Interrupt attention: 400 cycles per sample – $80\times$ less ✓.
- Sampling at a fixed rate fits polling only if the loop is dedicated; with any other work, interrupts win – the criterion is whether the CPU has anything else to do ✓.

3.2

- Per-word interrupts: $2048 \times 200 = 409\,600$ cycles ✓.
- DMA: $600 + 200 = 800$ cycles; ratio $409\,600/800 = 512\times$ ✓.
- Under 1% of $200 \times n$ cycles with one 800-cycle DMA bill: $800 < 0.01 \times 200n \Rightarrow n > 400$ words per interrupt ✓.
- Under DMA the CPU still pays the setup, the completion handling, and cache-coherence care – the data path, not the data movement ✓.

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