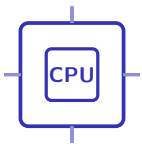
Hardware

IGCSE Computer Science ▪ Topic 3

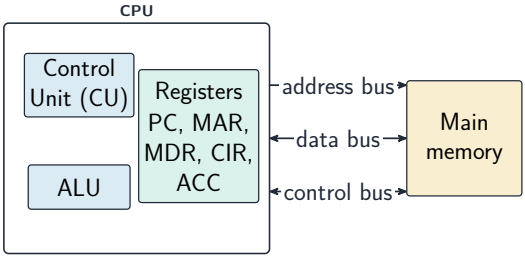
IGCSE Computer Science



What we will cover

1. The CPU & buses
2. The fetch–execute cycle
3. Input & output devices
4. RAM, ROM & storage
5. Virtual memory
6. Network hardware

Inside the CPU



3d printer

The special registers

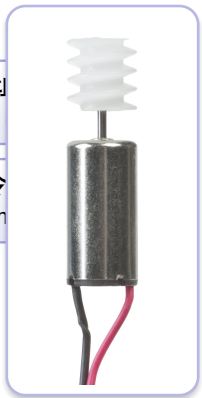
PC 程序计数器 – address of the *next* instruction

MAR 内存地址 – the address to

MDR 内存数据寄存器 – the data just fetched

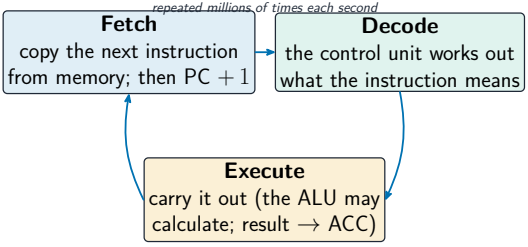
CIR 当前指令 – the instruction n

ACC 累加器 – the ALU's result



actuator motor

The fetch–execute cycle



barcode scanner

What makes a CPU faster

cores 核心
each runs instructions on its own – more do more at once

cache size
more data kept ready, so the CPU waits less

[illegible]

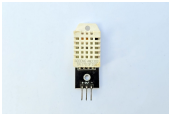
An **embedded system** 嵌入式系统 is a small computer built into a device to do one fixed job (a washing machine, a car engine).

cloud servers

Input and output devices

keyboard

mouse



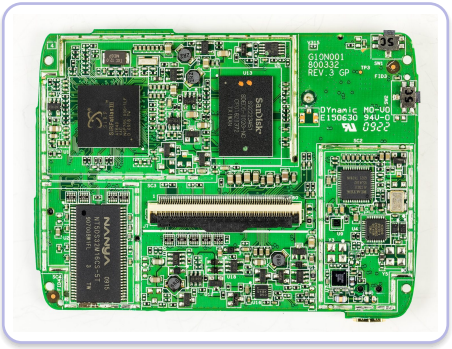
sensor

digital camera

Input sends data *into* the computer (keyboard, mouse, sensor, scanner); output sends it *out* (monitor, printer, speaker, actuator).

RAM vs ROM

	RAM	ROM
access	read & write	read only
power off	loses data	keeps data
	(volatile)	(non-volatile)
holds	programs in use	start-up code



embedded system

Secondary storage

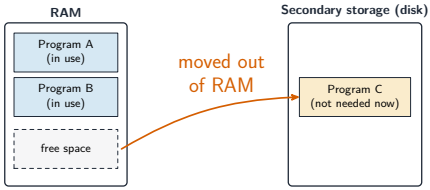
magnetic 磁存储
magnetised spots
on spinning disks
HDD, tape

optical 光存储
marks read by a laser
CD, DVD, Blu-ray

flatbed scanner

Secondary storage is non-volatile – it keeps data with the power off, unlike RAM.

Virtual memory



This frees RAM, so more programs can run than RAM alone could hold — but it is slower, because the disk is much slower than RAM.

hdd internal

Network hardware

- **NIC** 网络接口卡: the card that joins a device to a network
- **MAC address** 介质访问控制地址: identifies one physical device – fixed
- **IP address** 网际协议地址: identifies a device on a network – depends on the network
- **router** 路由器: connects networks (home → internet)

headphones

Topic 3 – key takeaways

1 CPU

ALU + CU + registers, joined by buses

2 Cycle

fetch → decode → execute, PC +1

3 Memory

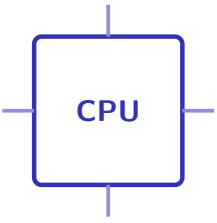
RAM volatile, ROM non-volatile; disk is secondary

4 Network

MAC fixed to device; IP set by the network

Check yourself

1. Which register holds the next instruction's address?
2. Is RAM volatile or non-volatile?
3. Which memory holds the start-up instructions?
4. Which address is fixed to the physical device?



Answers **1.** the PC **2.** volatile **3.** ROM **4.** the MAC address