

6(a)	One mark for each correct term in the correct place. The program counter stores the address of the next instruction to be processed. This address is then sent to the memory address register. This address is the location in RAM where the instruction can be found. The instruction is retrieved from RAM and immediately stored in the memory data register. The instruction is then sent to the current instruction register where it is decoded by the control unit. The instruction is decoded using an instruction set.
6(b)(i)	Hardware (interrupt)
6(b)(ii)	Interrupt handler // Interrupt service routine
6(b)(iii)	Any one from: - managing files - providing an interface - managing peripherals and drivers - managing memory - managing multitasking - providing a platform for running applications - providing system security - managing user accounts

4(a)	One mark for each correct part of the diagram. The diagram shows: - CIR is built into CU - CIR stores instruction - CU decodes the instruction - Instruction is decoded using an instruction set // Instruction is separated into opcode and operand - Signal is sent from CIR to ALU (to execute) - CU sends signal to RAM to fetch any data needed for instruction - ACC is built into ALU - ACC stores any data needed for instruction - ALU executes the instruction // ALU performs the mathematic/logical operation (needed by the instruction) Example:
4(b)	Any two from: - Independent/self-contained processing unit - It executes/processes instructions // It performs the FDE cycle - It contains registers/units (to process data)
4(c)	Four from (MAX 2 if no expansion given): - The number of cores could be increased // by example this means that more instructions can be processed simultaneously - The clock speed could be increased // by example this means that more instructions can be processed (by a core) per second - The cache could be increased // by example this means that more frequently used data/instructions can be stored (to be accessed faster than RAM)

5(a)	Any two from: - Program counter // PC - Memory address register // MAR - Memory data register // MDR - Current instruction register // CIR
5(b)	Any three from: CIR/CU receives the instruction from the MDR // Instruction sent from MDR to CIR/CU ... using the data bus - Instruction is separated into opcode and operand - Control unit decodes the instruction ... using an instruction set
5(c)	Any one from: - Accumulator - Memory address register // MAR - Memory data register // MDR
5(d)	- data - address - control
5(e)	- It can now execute more instructions/FDE per second ... this will increase the performance of the CPU
6(a)	Any one from: - Computer system that is designed to a perform dedicated/single function - Computer system that contains a microprocessor (and)/dedicated hardware - Computer system that is built into a larger system
6(b)	Assembler
6(c)	Any one from: - Convert to hexadecimal - Convert to denary - A character set can be used
6(d)	Any one from: - More control over manipulating the hardware - Faster execution for testing than a high-level language - They can use machine specific instructions
6(e)	Six from (MAX 4 for stating features): Code editor that allows the user to enter and amend code in their program Run-time environment ... that allows a program to be run and see the outputs of their program Error-diagnostic ... to show the programmer where there are errors in the program Auto-completion ... to give the user options/suggestions of key commands to select Auto-correction ... to correct a command that has a minor misspelling Prettyprint ... changes the colour of key commands so they are easy to identify

6	One mark for each correct term or definition in the correct place: Components - Control unit // CU - Memory address register // MAR - Data bus - Current instruction register // CIR Descriptions (Program counter) Stores the address of the next instruction to be fetched (Accumulator) Stores the interim result for a calculation
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3(a)	Any two from: - Program counter // PC - Memory address register // MAR - Current instruction register // CIR
3(b)	One mark for each correct part of the diagram. The diagram shows: - Data/Instruction sent from the MDR to the CIR/CU ... using the data bus ... the CIR that is built into the CU - Data/Instruction separated into operand and op code <u>Control unit/CU</u> decodes instruction ... using an instruction set For example: <pre> graph LR MDR[MDR] -- "Instruction sent using data bus" --> CIR[CIR] subgraph CU [Control unit] CIR end CU --> Decodes[Decodes instruction using instruction set] </pre>

5(a)	One mark for each correct term in the correct place: - address - memory address register // MAR - random access memory // RAM - memory data register // MDR - data - current instruction register // CIR - control unit // CU
5(b)	A list of (machine code) commands that can be processed by the CPU

8(a)	To process instructions/data To run the fetch–decode–execute cycle
8(b)(i)	Any one from: - To temporarily store data/instruction/address - To allow immediate access to data during the FDE cycle
8(b)(ii)	Any three from: - Memory address register // MAR - Memory data register // MDR - Accumulator // ACC - Program counter // PC - Current instruction register // CIR
8(c)	Any three from: - To execute instructions - To perform calculations // by example - To perform logical operations // by example - To store interim results of calculations - Stores/reads/writes data to/from the accumulator
8(d)	Any Four from: - It could have more cores ... increasing the number of FDE cycles/instructions it can perform at the same time - It could have a higher clock speed ... increasing the number of FDE cycles/instructions per second it can perform - It could have a greater cache size ... meaning more frequently used data can be accessed faster

2(a)	One mark for letter and One mark for matching correction. - Statement BMAR stores addresses and not instructions - Statement CData is from bus not PC // Data is from address in MAR not PC
2(b)(i)	It can run 3.5 billion FE cycles each second // it can execute 3.5 billion instructions each second
2(b)(ii)	Any two from: More cores increases/improves the performance More cores mean more FDE cycles/instructions are executed each second ...because each core runs an FE cycle/instruction simultaneously
2(b)(iii)	Any two from: More cache improves performance ...because more cache means the processor can access more frequently used data/instructions faster ...instead of having to access the data from the slower-access RAM
2(c)(i)	Any two from: - Volatile storage - Stores data for the processor to access directly/quickly // directly accessed by the CPU - Stores currently running data/instructions
2(c)(ii)	Any one from: e.g. - BIOS // bootstrap/loader - Firmware - Parts of OS
2(c)(iii)	Any one from: e.g. - To run programs when there is insufficient RAM to run them - To allow RAM to store more data when required

1(a)	– A
1(b)	– C
1(c)	– Control unit
1(d)	Any two from: (The CPU completes) 2.4 billion ... cycles/clock pulses per second
1(e)(i)	Any two from: - Stores data that has been fetched/to be written to memory
1(e)(ii)	Any three from: - Memory address register // MAR - Program counter // PC - Current instruction register // CIR - Accumulator // ACC

3(a)(i)	– The maximum number of FDE cycles/instructions a CPU can perform/process/execute in a second
3(a)(ii)	– Increases/improves the performance // Tasks can be performed quicker/faster – ... because more FDE cycles/instructions can be processed in a second
3(b)	– Stores addresses ... – ... of next instruction/data to be fetched // where data is to be written to
3(c)	– Instruction set
4(a)	Any two from: - Performs a single/limited/dedicated function/task - It has a microprocessor - It has dedicated hardware - Uses firmware - It is normally built into a larger device/system - User normally cannot reprogram - It does not require much power - It is cheap to manufacture - Works automatically // works without human intervention - It is small (in size) - It is a real-time system
4(b)	One mark for each correct system: - security light system - freezer - vending machine