Solutions

Each answer shows the steps, then the **result**.

2.1

- ALU stands for Arithmetic and Logic Unit
- it carries out **calculations and logical operations**

2.2

- the cycle has three named stages
- **fetch**, **decode**, **execute**

2.3

- the next instruction's address is held in the **program counter (PC)**

2.4

- both directions: **data bus**
- one direction (CPU → memory): **address bus**

2.5

- cache is very fast memory holding frequently used instructions and data close to the CPU
- the CPU makes fewer slow fetches from RAM, so it **spends less time waiting**

3.1 B

- cache is **very fast memory holding frequently used data**
- A is ROM/storage; C is false; D is secondary storage

3.2

(a)

- any **two** of: **more cores** / **larger cache** / **higher clock speed**

(b)

- a small computer built into a device to do **one fixed job**
- e.g. a **washing machine** or **microwave**

3.3

(a)

- **PC**: program counter — address of the next instruction
- **MAR**: memory address register — address being read or written
- **MDR**: memory data register — data or instruction from that address
- **ACC**: accumulator — result of a calculation

(b)

- address in the PC is copied to the MAR
- the PC is incremented
- the instruction at that address is fetched into the MDR along the data bus
- it is copied from the MDR into the CIR ready for decoding

(c)

- a "write" signal uses the **control bus**
- it is bidirectional because the CPU sends commands while devices send back signals such as an interrupt request

(d)

- not all programs can be split into parts that run at the same time
- cores still share memory and wait for each other, so extra cores are **not always fully used**

(e)

- e.g. a **washing-machine controller**, traffic lights, a microwave, or a car engine unit
- it is built into a larger device and runs **one dedicated program** the user cannot change