Past-paper walk-through

Computer architecture ▪ 3.1

eXercise

Questions in this set

- 0478/11 N25 Q6 ▪ 9 marks
- 0478/12 N25 Q4 ▪ 11 marks
- 0478/11 N24 Q5 ▪ 11 marks
- 0478/11 N24 Q6 ▪ 10 marks
- 0478/12 N24 Q6 ▪ 6 marks
- 0478/13 N24 Q3 ▪ 6 marks
- 0478/12 J24 Q5 ▪ 8 marks
- 0478/13 J24 Q8 ▪ 13 marks
- 0478/12 M24 Q2 ▪ 13 marks
- 0478/11 N23 Q1 ▪ 10 marks

Questions in this set

- 0478/12 N23 Q3 ▪ 6 marks
- 0478/12 N23 Q4 ▪ 5 marks

Reading the mark scheme

- **B1** a mark that stands on its own – the point is either made or not.
- **M1** a *method* mark: the right approach, even if the number is wrong.
- **A1** an *answer* mark, and it usually needs its M mark first.
- **C1** a working mark on the way to the answer.
- // separates answers the examiner accepts equally.
- **ecf** = error carried forward: a later part is marked on your own earlier answer.
- **owtte** = "or words to that effect" – the wording need not match.

Question 6

0478/11 N25 ▪ Q6 ▪ 9 marks

A computer with a Von Neumann architecture has a central processing unit (CPU).

(a) Complete the statements about the operation of the CPU.

Use the terms from the list. **Not** all terms will need to be used. You should only use each term once.

- accumulator
- arithmetic logic unit
- character set
- control unit
- current instruction register
- cipher

Question 6

- decoding set
- instruction counter
- instruction set
- memory address register
- memory data register
- memory instruction register
- next instruction register
- program counter
- program register

Question 6

The ___ stores the address of the next instruction to be fetched. This address is then sent to the ___. This address is the location in RAM where the instruction can be found. The instruction is retrieved from RAM and immediately stored in the ___. The instruction is then sent to the ___ where it is decoded by the ___. The instruction is decoded using an ___. **[6]**

Question 6

0478/11 N25 ▪ Q6 ▪ 9 marks

A computer with a Von Neumann architecture has a central processing unit (CPU).

(b)(i) An interrupt is sent to the CPU every time a key is pressed on the keyboard. Give the name of this type of interrupt. **[1]**

(b)(ii) Give the name of the program that services the interrupt. **[1]**

(b)(iii) Give **one** other function of an operating system. **[1]**

Solution 6

(a) Mark scheme

- One mark for each correct term in the correct place.
- The program counter stores the address of the next instruction to be processed. This address is then sent to the memory address register. This address is the location in RAM where the instruction can be found. The instruction is retrieved from
- RAM and immediately stored in the memory data register. The instruction is then sent to the current instruction register where it is decoded by the control unit. The instruction is decoded using an instruction set.

Solution 6

(b)(i)

Mark scheme

- Hardware (interrupt)

(b)(ii)

Mark scheme

- Interrupt handler // Interrupt service routine

Solution 6

(b)(iii) Mark scheme

- Any one from:
- ▪ managing files
- ▪ providing an interface
- ▪ managing peripherals and drivers
- ▪ managing memory
- ▪ managing multitasking
- ▪ providing a platform for running applications
- ▪ providing system security

Solution 6

- managing user accounts

Question 4

0478/12 N25 ▪ Q4 ▪ 11 marks

A computer with a Von Neumann architecture has a central processing unit (CPU) that performs the fetch–decode–execute (FDE) cycle.

(a) Complete and annotate the diagram to show how instructions are decoded and executed.

control unit (CU)

arithmetic logic unit (ALU) **[5]**

(b) The CPU is dual core and has a processor speed of 2.4 GHz.

Describe what is meant by a core. **[2]**

(c) Explain **two** ways that the performance of the CPU could be increased. **[4]**

Solution 4

(a) Mark scheme

- One mark for each correct part of the diagram.
- The diagram shows:
- ▪ CIR is built into CU
- ▪ CIR stores instruction
- ▪ CU decodes the instruction
- ▪ Instruction is decoded using an instruction set // Instruction is separated into opcode and operand
- ▪ Signal is sent from CIR to ALU (to execute)

Solution 4

- ▪ CU sends signal to RAM to fetch any data needed for instruction
- ▪ ACC is built into ALU
- ▪ ACC stores any data needed for instruction
- ▪ ALU executes the instruction // ALU performs the mathematic/logical operation (needed by the instruction)
- Example:

Solution 4

(b) Mark scheme

- Any two from:
- ▪ Independent/self-contained processing unit
- ▪ It executes/processes instructions // It performs the FDE cycle
- ▪ It contains registers/units (to process data)
- 2 control unit (CU) arithmetic logic unit (ALU)
- CIR
- ACC
- Instruction is stored in CIR

Solution 4

- CU uses an instruction set to decode instruction and sends a signal to ALU to execute the instruction
- ACC stores data needed to execute instruction

Solution 4

(c) Mark scheme

- Four from (MAX 2 if no expansion given):
- ▪ The number of cores could be increased // by example ...
- ▪ ... this means that more instructions can be processed simultaneously
- ▪ The clock speed could be increased // by example ...
- ▪ ... this means that more instructions can be processed (by a core) per second
- ▪ The cache could be increased // by example ...
- ▪ ... this means that more frequently used data/instructions can be stored (to be accessed faster than RAM)

Question 5

0478/11 N24 ▪ Q5 ▪ 11 marks

A central processing unit (CPU) performs the fetch–decode–execute (FDE) cycle.

(a) Give the name of **two** registers that are used in the fetch stage of the cycle.

1. 2. **[2]**

Question 5

0478/11 N24 ▪ Q5 ▪ 11 marks

A central processing unit (CPU) performs the fetch–decode–execute (FDE) cycle.

(b) Describe what happens at the decode stage of the cycle. **[3]**

Question 5

0478/11 N24 ▪ Q5 ▪ 11 marks

A central processing unit (CPU) performs the fetch–decode–execute (FDE) cycle.

(c) Give **one** register in the CPU that is used in the execute stage of the cycle. **[1]**

Question 5

0478/11 N24 ▪ Q5 ▪ 11 marks

A central processing unit (CPU) performs the fetch–decode–execute (FDE) cycle.

(d) Buses are used in the CPU to transmit data through the FDE cycle.

Circle **three** buses that are used in the CPU. **[3]**

A fetch

B address

C register

D execute

E data

F decode

Question 5

G calculation

H central

I value

J binary

K control

Question 5

0478/11 N24 ▪ Q5 ▪ 11 marks

A central processing unit (CPU) performs the fetch–decode–execute (FDE) cycle.

(e) A user changes their CPU from one with a dual core and a clock speed of 2.4 GHz to one with a dual core and a clock speed of 3.5 GHz.

Explain the effect this change will have on the performance of the CPU. **[2]**

Solution 5

(a)

Mark scheme

- Any two from:
- ▪ Program counter // PC
- ▪ Memory address register // MAR
- ▪ Memory data register // MDR
- ▪ Current instruction register // CIR

Solution 5

(b)

Mark scheme

- Any three from:
- ▪ CIR/CU receives the instruction from the MDR // Instruction sent from MDR to CIR/CU
- ▪ ... using the data bus
- ▪ Instruction is separated into opcode and operand
- ▪ Control unit decodes the instruction
- ▪ ... using an instruction set

Solution 5

(c)

Mark scheme

- Any one from:
- ▪ Accumulator
- ▪ Memory address register // MAR
- ▪ Memory data register // MDR

Solution 5

(d)

Mark scheme

- data
- address
- control

Solution 5

(e)

Mark scheme

- It can now execute more instructions/FDE per second
- ... this will increase the performance of the CPU

Question 6

0478/11 N24 ▪ Q6 ▪ 10 marks

A computer programmer uses assembly language to create a computer program for an embedded system in a washing machine.

(a) State what is meant by an embedded system. **[1]**

(b) Give the name of the translator that will be used for the program. **[1]**

(c) The washing machine needs to display error codes on a small screen if there is a problem with the washing machine.

The error codes are stored as binary. The binary numbers are too long to be displayed on the washing machine.

State how the error codes could be reduced in length to be displayed on the screen. **[1]**

(d) Give **one** benefit to the programmer of using assembly language to write the program. **[1]**

Question 6

(e) The programmer uses an integrated development environment (IDE) to write the program.
A built-in translator to convert the program into machine code is one way that the IDE helps the computer programmer.
Describe **three** other ways the IDE can help the programmer. **[6]**

Solution 6

(a)

Mark scheme

- Any one from:
- ▪ Computer system that is designed to a perform dedicated/single function
- ▪ Computer system that contains a microprocessor (and)/dedicated hardware
- ▪ Computer system that is built into a larger system

Solution 6

(b)

Mark scheme

- Assembler

Solution 6

(c)

Mark scheme

- Any one from:
- ▪ Convert to hexadecimal
- ▪ Convert to denary
- ▪ A character set can be used

Solution 6

(d)

Mark scheme

- Any one from:
- ▪ More control over manipulating the hardware
- ▪ Faster execution for testing than a high-level language
- ▪ They can use machine specific instructions

Solution 6

(e) Worked steps

Six marks are available but **at most four for merely stating features** — so every feature must be paired with **what it does for the programmer**, and the marks come in pairs.

Features that help while **writing**:

- **Code editor** — lets the user enter and amend the program's code.
- **Auto-complete / context-sensitive prompts** — suggests the rest of a keyword or the parameters a routine expects.
- **Auto-correction and dynamic syntax checking** — flags a mistyped keyword as the line is typed rather than at compile time.

Solution 6

- **Prettyprint / auto-indentation and syntax highlighting** — colours keywords and indents blocks so the structure is visible.

Features that help while **running and testing**:

- **Run-time environment** — runs the program from inside the IDE without leaving it.
- **Translator** — an interpreter for line-by-line checking, or a compiler for the finished program.
- **Error diagnostics / report window** — reports the type of error and the line it is on.
- **Breakpoints and single stepping** — stop execution at a chosen line, or run one line at a time, watching the variables change.

Solution 6

Write each as **feature — what it does**. A bare list of eight names caps at four marks; four properly explained pairs reach six.
The pairing to notice: the writing features stop errors being made, and the running features find the ones that were. **Mark scheme**

- Six from (MAX 4 for stating features):
- Code editor ...
- ... that allows the user to enter and amend code in their program
- Run-time environment
- ... that allows a program to be run and see the outputs of their program
- Error-diagnostic

Solution 6

- ... to show the programmer where there are errors in the program
- Auto-completion
- ... to give the user options/suggestions of key commands to select
- Auto-correction
- ... to correct a command that has a minor misspelling
- Prettyprint
- ... changes the colour of key commands do they are easy to identify

Question 6

0478/12 N24 ▪ Q6 ▪ 6 marks

The table contains names and descriptions of components in a central processing unit (CPU). Complete the table by giving the missing component names and descriptions.

Component name	**Description**
	sends signals to manage the flow of data through the CPU
program counter	
	stores the address of the data that is about to be fetched from random access memory (RAM) into the CPU
	transmits data between the RAM and the CPU
accumulator	
	stores an instruction when it is being decoded

Question 6

[6]

Question 6

Component name	Description
.....	sends signals to manage the flow of data through the CPU
program counter	....
.....	stores the address of the data that is about to be fetched from random access memory (RAM) into the CPU
.....	transmits data between the RAM and the CPU
accumulator	....
	stores an instruction when it is being decoded

Question 6

.....	stores an instruction when it is being decoded

[6]

Solution 6

- One mark for each correct term or definition in the correct place:
- Components
- ▪ Control unit // CU
- ▪ Memory address register // MAR
- ▪ Data bus
- ▪ Current instruction register // CIR
- Descriptions
- ▪ (Program counter) Stores the address of the next instruction to be fetched

Solution 6

- ▪ (Accumulator) Stores the interim result for a calculation

Question 3

0478/13 N24 ▪ Q3 ▪ 6 marks

An instruction is fetched from random access memory (RAM) into the memory data register (MDR) to be decoded.

(a) Identify **two** other registers that are used in the fetch stage of the cycle.

1. 2. **[2]**

Question 3

0478/13 N24 ▪ Q3 ▪ 6 marks

An instruction is fetched from random access memory (RAM) into the memory data register (MDR) to be decoded.

(b) Complete and annotate the diagram to show how the data is decoded once it has been fetched into the MDR.

Question 3

[4]

Solution 3

(a)

Mark scheme

Any two from:

- Program counter // PC
- Memory address register // MAR
- Current instruction register // CIR

Solution 3

(b) Mark scheme

One mark for each correct part of the diagram.
The diagram shows:

- Data/Instruction sent from the MDR to the CIR/CU
- ...using the data bus
- ...the CIR that is built into the CU
- Data/instruction separated into operand and op code
- Control unit/CU decodes instruction
- ...using an instruction set

For example:

Question 5

0478/12 J24 ▪ Q5 ▪ 8 marks

Instructions are processed by a central processing unit (CPU) in a computer.

(a) Complete the paragraph about fetching an instruction into the CPU to be processed.

Use the terms from the list.

Some of the terms in the list will **not** be used. You should only use a term once.

- address
- arithmetic logic unit (ALU)
- binary
- control unit (CU)
- current instruction register (CIR)
- data

Question 5

- denary
- driver
- fetch
- interrupt
- memory address register (MAR)
- memory data register (MDR)
- random access memory (RAM)
- read only memory (ROM)
- secondary storage
- signal

Question 5

The program counter contains the ___ of the next instruction to be processed; this is then sent to the ___ using the address bus. The address is then sent to the ___. Once the address is received, the instruction stored at the location is sent to the ___, using the ___ bus. The instruction is then sent to the ___ that is built into the ___.**[7]**

Question 5

0478/12 J24 ▪ Q5 ▪ 8 marks

Instructions are processed by a central processing unit (CPU) in a computer.

(b) The CPU uses an instruction set to decode the instruction.

State what is meant by an instruction set. **[1]**

Solution 5

(a) Mark scheme

- One mark for each correct term in the correct place:
- ▪ address
- ▪ memory address register // MAR
- ▪ random access memory // RAM
- ▪ memory data register // MDR
- ▪ data
- ▪ current instruction register // CIR
- ▪ control unit // CU

Solution 5

(b)

Mark scheme

- A list of (machine code) commands that can be processed by the CPU

Question 8

0478/13 J24 ▪ Q8 ▪ 13 marks

A student has a computer that has a central processing unit (CPU).

(a) Describe the role of the CPU in the computer. **[2]**

(b)(i) State the purpose of a register. **[1]**

(b)(ii) Give **three** registers that are built into the CPU.

1. 2. 3. **[3]**

(c) One component in the CPU is the arithmetic logic unit (ALU).

Describe the purpose of the ALU. **[3]**

(d) The student wants to replace the CPU to increase the performance of the computer.

Explain why a different CPU can increase the performance. **[4]**

Solution 8

(a)

Mark scheme

- To process instructions/data
- To run the fetch–decode–execute cycle

Solution 8

(b)(i)

Mark scheme

- Any one from:
- ▪
- To temporarily store data/instruction/address
- ▪
- To allow immediate access to data during the FDE cycle

Solution 8

(b)(ii) Mark scheme

- Any three from:
- ▪
- Memory address register // MAR
- ▪
- Memory data register // MDR
- ▪
- Accumulator // ACC
- ▪

Solution 8

- Program counter // PC
- ▪
- Current instruction register // CIR

Solution 8

(c) Mark scheme

- Any three from:
- ▪
- To execute instructions
- ▪
- To perform calculations // by example
- ▪
- To perform logical operations // by example
- ▪

Solution 8

- To store interim results of calculations
- ▪
- Stores/reads/writes data to/from the accumulator

Solution 8

(d) Mark scheme

- Any Four from:
- ▪
- It could have more cores
- ▪
- ... increasing the number of FDE cycles/instructions it can perform at the same time
- ▪
- It could have a higher clock speed

Solution 8

- ▪
- ... increasing the number of FDE cycles/instructions per second it can perform
- ▪
- It could have a greater cache size
- ▪
- ... meaning more frequently used data can be accessed faster

Question 2

0478/12 M24 ▪ Q2 ▪ 13 marks

A computer has a central processing unit (CPU).
The CPU includes the registers:

- Program counter (PC)
- Memory address register (MAR)
- Memory data register (MDR)
- Accumulator (ACC)
- Current instruction register (CIR).

Question 2

(a) The table contains **five** statements about the role of registers in the fetch–decode–execute cycle of a CPU.

Letter	Statement
A	PC stores the address of the next instruction to be accessed
B	MAR stores the instructions of the program that is running
C	MDR stores the data passed to it from the PC
D	ACC stores the result of each calculation
E	CIR stores the instruction currently being executed

Question 2

Two of the statements are **not** correct.
Identify the letter of each incorrect statement.
Suggest a corrected statement for each.
Incorrect statement 1
Corrected statement

Incorrect statement 2
Corrected statement **[4]**

Question 2

Letter	Statement
A	PC stores the address of the next instruction to be accessed
B	MAR stores the instructions of the program that is running
C	MDR stores the data passed to it from the PC
D	ACC stores the result of each calculation
E	CIR stores the instruction currently being executed

Question 2

0478/12 M24 ▪ Q2 ▪ 13 marks

A computer has a central processing unit (CPU).
The CPU includes the registers:

- Program counter (PC)
- Memory address register (MAR)
- Memory data register (MDR)
- Accumulator (ACC)
- Current instruction register (CIR).

Question 2

(b)(i) State what is meant by a 3.5 GHz processor. **[1]**

(b)(ii) The CPU is changed to a dual-core 3.5 GHz processor.
Explain how the number of cores affects the performance of a CPU. **[2]**

(b)(iii) The amount of cache is increased to 64 kB.
Explain how the amount of cache affects the performance of a computer. **[2]**

Question 2

0478/12 M24 ▪ Q2 ▪ 13 marks

A computer has a central processing unit (CPU).
The CPU includes the registers:

- Program counter (PC)
- Memory address register (MAR)
- Memory data register (MDR)
- Accumulator (ACC)
- Current instruction register (CIR).

Question 2

(c)(i) Random access memory (RAM) is one example of primary storage.
Describe what is meant by RAM. **[2]**

(c)(ii) Read only memory (ROM) is another example of primary storage. ROM often stores the start-up instructions for a computer.
Identify **one** other item of data that is commonly stored in ROM. **[1]**

(c)(iii) Some computers make use of virtual memory.
State the purpose of virtual memory. **[1]**

Solution 2

(a)

Mark scheme

- One mark for letter and One mark for matching correction.
- ▪ Statement B ...
- ▪ ...MAR stores addresses and not instructions
- ▪ Statement C ...
- ▪ ...Data is from bus not PC //
- Data is from address in MAR not PC

Solution 2

(b)(i)

Mark scheme

- It can run 3.5 billion FE cycles each second // it can execute 3.5 billion instructions each second

Solution 2

(b)(ii)

Mark scheme

- Any two from:
- ▪ More cores increases/improves the performance
- ▪ More cores mean more FDE cycles/instructions are executed each second
- ▪ ...because each core runs an FE cycle/instruction simultaneously

Solution 2

(b)(iii)

Mark scheme

- Any two from:
- ▪ More cache improves performance
- ▪ ...because more cache means the processor can access more frequently used data/instructions faster
- ▪ ...instead of having to access the data from the slower-access RAM

Solution 2

(c)(i)

Mark scheme

- Any two from:
- ▪ Volatile storage
- ▪ Stores data for the processor to access directly/quickly // directly accessed by the CPU
- ▪ Stores currently running data/instructions

Solution 2

(c)(ii)

Mark scheme

- Any one from:
- e.g.
- ▪ BIOS // bootstrap/loader
- ▪ Firmware
- ▪ Parts of OS

Solution 2

(c)(iii)

Mark scheme

- Any one from:
- e.g.
- ▪ To run programs when there is insufficient RAM to run them
- ▪ To allow RAM to store more data when required

Question 1

0478/11 N23 ▪ Q1 ▪ 10 marks

1 A student uses a computer and several hardware devices to complete his schoolwork.

The computer has a central processing unit (CPU).

(a) The student uses a keyboard to complete his schoolwork.

Tick (✓) **one** box to show which type of device the keyboard is.

A input ☐

B memory ☐

C output ☐

D storage ☐

[1]

Question 1

(b) The student uses a printer to print his schoolwork.

Tick (✓) **one** box to show which type of device the printer is.

A input ☐

B memory ☐

C output ☐

D storage ☐

[1]

(c) A component in the CPU sends signals to manage the fetch-decode-execute cycle.

State the name of this component.

Question 1

(d) The CPU has a clock speed of 2.4 Ghz.

Describe what is meant by a 2.4 Ghz clock speed.

Question 1

(e) The CPU contains registers including the memory data register (MDR).

(i) Describe the role of the MDR in the fetch-decode-execute cycle.

Question 1

(ii) Identify **three** other registers contained in the CPU.

Question 1

[3]

Solution 1

(a)

Mark scheme

- —
- A
- 1

Solution 1

(b)

Mark scheme

- —
- C
- 1

Solution 1

(c)

Mark scheme

- –
- Control unit
- 1

Solution 1

(d)

Mark scheme

- Any two from:
- –
- (The CPU completes) 2.4 billion
- –
- ... cycles/clock pulses per second
- 2

Solution 1

(e)(i)

Mark scheme

- Any two from:
- –
- Stores data ...
- –
- ... that has been fetched/to be written to memory
- 2

Solution 1

(e)(ii) Mark scheme

- Any three from:
- –
- Memory address register // MAR
- –
- Program counter // PC
- –
- Current instruction register // CIR
- –

Solution 1

- Accumulator // ACC

Question 3

0478/12 N23 ▪ Q3 ▪ 6 marks

3 A user's computer has a central processing unit (CPU) that has a clock speed of 2 GHz.

She wants to change it to a CPU that has a clock speed of 3 GHz.

(a) (i) State what is meant by clock speed.

Question 3

(ii) Explain the effect this change will have on the performance of the CPU.

Question 3

(b) The CPU contains a memory address register (MAR).

Describe the role of the MAR in the fetch–decode–execute cycle.

Question 3

(c) The CPU has a list of all the machine code commands it can process.

State the name of this list of commands.

Solution 3

(a)(i)

Mark scheme

- –
- The maximum number of FDE cycles/instructions a CPU can
- perform/process/execute in a second
- 1

Solution 3

(a)(ii)

Mark scheme

- –
- Increases/improves the performance // Tasks can be performed
- quicker/faster
- –
- ... because more FDE cycles/instructions can be processed in a second
- 2

Solution 3

(b)

Mark scheme

- –
- Stores addresses ...
- –
- ... of next instruction/data to be fetched // where data is to be written to
- 2

Solution 3

(c)

Mark scheme

- —
- Instruction set
- 1
- 0478/12
- October/November
- 2023

Question 4

0478/12 N23 ▪ Q4 ▪ 5 marks

4 A washing machine is an example of an embedded system.

(a) Give **two** characteristics of an embedded system.

Question 4

[2]

(b) Circle **three** other examples of an embedded system.

freezer laptop

personal computer (PC) security light system smartphone

vending machine web server

[3]

Solution 4

(a) Mark scheme

- Any two from:
- –
- Performs a single/limited/dedicated function/task
- –
- It has a microprocessor
- –
- It has dedicated hardware
- –

Solution 4

- Uses firmware
- —
- It is normally built into a larger device/system
- —
- User normally cannot reprogram
- —
- It does not require much power
- —
- It is cheap to manufacture
- —

Solution 4

- Works automatically // works without human intervention
- –
- It is small (in size)
- –
- It is a real-time system
- 2

Solution 4

(b) Mark scheme

- One mark for each correct system:
- —
- security light system
- —
- freezer
- —
- vending machine
- 3