15. Hardware and Virtual Machines — Starter Quiz · 课前小测

A-Level Computer Science Name: _____ Score: _____

1. A RISC processor is characterised by:

   ☐ a small set of simple, fixed-length instructions

   ☐ many complex variable-length instructions

   ☐ no registers

   ☐ instructions that each take many cycles

2. SIMD means:

   ☐ one instruction operates on many data items at once

   ☐ many instructions on one data item

   ☐ one instruction on one data item

   ☐ no instructions at all

3. By the absorption law, A + A · B simplifies to _____.

   _____

4. In a half adder, the sum output S is produced by which gate?

   ☐ XOR

   ☐ AND

   ☐ OR

   ☐ NOT

5. In a RISC processor, the only instructions that access memory are load and _____.

   _____

6. A massively parallel computer uses:

   ☐ thousands of processors with their own memory, exchanging messages

   ☐ a single very fast core

   ☐ one processor and a huge disk

   ☐ no network

7. By De Morgan's law, $\overline{A \cdot B}$ equals:

   ☐ $\overline{A} + \overline{B}$

   ☐ $\overline{A} \cdot \overline{B}$

   ☐ $A + B$

   ☐ $A \cdot B$

8. In a half adder the carry output C is produced by which single gate?

   _____

9. Applying De Morgan's law to an expression involves which steps? Select **all** that apply.

   ☐ remove the bar over the whole expression

   ☐ swap AND for OR, or OR for AND

   ☐ negate each operand individually

   ☐ reverse the order of the operands

   Tick every correct option.

10. A system VM (managed by a hypervisor) runs a whole guest operating system, whereas a process VM like the JVM just runs one program's portable bytecode.

    ☐ True ☐ False

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Answers · 答案

A-Level Computer Science

1. **a small set of simple, fixed-length instructions**

   RISC keeps instructions few, simple and fixed-length (usually 1 cycle); CISC has many complex variable-length ones.

2. **one instruction operates on many data items at once**

   Single Instruction, Multiple Data — e.g. a GPU running the same operation on thousands of pixels.

3. **A**

   If A is true the whole expression is true whatever B is, and if A is false both terms are false. B cannot affect the result.

4. **XOR**

   $S = A$ XOR B (1 when the inputs differ); the carry is A AND B.

5. **store**

   Everything else is register to register. That restriction is what makes instructions fixed-length, uniform in timing and easy to pipeline.

6. **thousands of processors with their own memory, exchanging messages**

   Massively parallel systems (supercomputers) link thousands of processors with distributed memory over a fast network.

7. $\overline{A} + \overline{B}$

   Negate the whole, swap AND→OR, negate each operand: $\overline{A \cdot B} = \overline{A} + \overline{B}$.

8. **AND**

   C is 1 only when both inputs are 1, which is AND. The sum S is 1 when exactly one input is 1, which is XOR.

9. **remove the bar over the whole expression; swap AND for OR, or OR for AND; negate each operand individually**

   Negate the whole, swap the operator, negate each part. Order is irrelevant, since AND and OR are commutative.

10. **True**

    System VMs share one physical machine among several guest OSes; process VMs give ”write once, run anywhere” for a single program.