15. Hardware and Virtual Machines

Starter Quiz · 课前小测

A-Level Computer Science Name: _____ Score: _____

1. A RISC processor is characterised by:

   ☐ a small set of simple, fixed-length instructions

   ☐ many complex variable-length instructions

   ☐ no registers

   ☐ instructions that each take many cycles

2. SIMD means:

   ☐ one instruction operates on many data items at once

   ☐ many instructions on one data item

   ☐ one instruction on one data item

   ☐ no instructions at all

3. By De Morgan's law, $\overline{A \cdot B}$ equals:

   ☐ $\overline{A} + \overline{B}$

   ☐ $\overline{A} \cdot \overline{B}$

   ☐ $A + B$

   ☐ $A \cdot B$

4. In a half adder, the sum output S is produced by which gate?

   ☐ XOR

   ☐ AND

   ☐ OR

   ☐ NOT

5. When a pipeline is full, it completes about:

   ☐ one instruction per clock cycle

   ☐ one instruction every five cycles

   ☐ all instructions at once

   ☐ no instructions

6. A data hazard stalls the pipeline when an instruction needs a result that is not ready yet; a control hazard comes from a branch changing which instruction runs next.

   ☐ True ☐ False

7. A system VM (managed by a hypervisor) runs a whole guest operating system, whereas a process VM like the JVM just runs one program's portable bytecode.

   ☐ True ☐ False

8. In a Karnaugh map, a larger group of adjacent 1s eliminates more variables, giving a simpler term (a group of 2 drops one variable, a group of 4 drops two).

   ☐ True ☐ False

9. A flip-flop is bistable — it has two stable states and remembers one bit — which makes it the building block of registers and SRAM.

   ☐ True ☐ False

10. A massively parallel computer uses:

    ☐ thousands of processors with their own memory, exchanging messages

    ☐ a single very fast core

    ☐ one processor and a huge disk

    ☐ no network

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Answers · 答案

A-Level Computer Science

1. **a small set of simple, fixed-length instructions**

   RISC keeps instructions few, simple and fixed-length (usually 1 cycle); CISC has many complex variable-length ones.

2. **one instruction operates on many data items at once**

   Single Instruction, Multiple Data — e.g. a GPU running the same operation on thousands of pixels.

3. $\overline{A} + \overline{B}$

   Negate the whole, swap AND→OR, negate each operand: $\overline{A \cdot B} = \overline{A} + \overline{B}$.

4. **XOR**

   $S = A$ XOR B (1 when the inputs differ); the carry is A AND B.

5. **one instruction per clock cycle**

   Overlapping the stages means a new instruction finishes each cycle once the pipeline is full.

6. **True**

   Hazards force the pipeline to stall (or flush), which is why they reduce the ideal one-per-cycle throughput.

7. **True**

   System VMs share one physical machine among several guest OSes; process VMs give ”write once, run anywhere” for a single program.

8. **True**

   You group adjacent 1s into power-of-two rectangles in Gray-code order; the bigger the group, the simpler the term it becomes.

9. **True**

   Chaining flip-flops gives registers and counters; SRAM cache is built from them (no refresh needed, unlike DRAM).

10. **thousands of processors with their own memory, exchanging messages**

    Massively parallel systems (supercomputers) link thousands of processors with distributed memory over a fast network.