

4(a)	1 mark for: LSL #2								
4(b)	<table><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	1		
4(c)	<table><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr></table>	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1		
4(d)	<table><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr></table>	1	1	1	1	0	0	1	1
1	1	1	1	0	0	1	1		

3(a)(i)	1 mark The value of the operand is an offset value which is added to another base value to give the address from which the contents are loaded to the accumulator								
3(a)(ii)	1 mark per bullet point, max 2 marks - Program counter (PC) - Memory Data Register (MDR) - Memory Address Register (MAR) - Current Instruction Register (CIR) - Status Register								
3(b)	1 mark for each correct value, max 3 marks <table border="1"> <thead> <tr> <th>Instruction</th><th>Value in ACC</th></tr> </thead> <tbody> <tr> <td>LDM #98</td><td>98</td></tr> <tr> <td>LDI 101</td><td>8</td></tr> <tr> <td>LDX 100</td><td>32</td></tr> </tbody> </table>	Instruction	Value in ACC	LDM #98	98	LDI 101	8	LDX 100	32
Instruction	Value in ACC								
LDM #98	98								
LDI 101	8								
LDX 100	32								
3(c)	1 mark per bullet point, max 2 marks for each Clock Speed: - Processor can perform more F-E cycles per second ... so more instructions / data can be processed each second Cache Memory: - Can store more of the most frequently used instructions ... which reduces the need to access slower RAM								

6(a)	1 mark for each correct row <table><tr><th>Current contents of the ACC</th><th>Instruction</th><th>Contents of the ACC after the execution of the instruction</th></tr><tr><td>0000 1111</td><td>AND 101</td><td>0000 1110</td></tr><tr><td>0000 0000</td><td>LDM #100</td><td>0110 0100</td></tr><tr><td>0000 0001</td><td>XOR &F1</td><td>1111 0000</td></tr><tr><td>0001 0001</td><td>CMP 101</td><td>0001 0001</td></tr></table>	Current contents of the ACC	Instruction	Contents of the ACC after the execution of the instruction	0000 1111	AND 101	0000 1110	0000 0000	LDM #100	0110 0100	0000 0001	XOR &F1	1111 0000	0001 0001	CMP 101	0001 0001
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0000 0000	LDM #100	0110 0100														
0000 0001	XOR &F1	1111 0000														
0001 0001	CMP 101	0001 0001														
6(b)	1 mark for each bullet point, max 4 marks • MAR stores the <u>address</u> of the next instruction / data to be read from / or written to memory • The address is received from the Program Counter (PC) • The MDR stores the data / instruction in the address stored in the MAR which has been read / written • The instruction passes to the CIR for decoding and executing															
6(c)	1 mark for each bullet point, max 3 marks • Data movement • Arithmetic operations • Conditional and unconditional (jump) instructions															

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One mark per mark point (Max 7)

MP1 LDD 300 seen
 MP2 Correct use of STO seen (at least once)
 MP3 Correct use of LDD 420 seen
 MP4 Correct use of LDI B
 MP5 Correct use of ADD A

Opcode	Operand
LDD	300
STO	A
LDD	420
STO	B
LDI	B
ADD	A
STO	Answer

MP6 Correct labelling of three addresses A:, B: and Answer:
 MP7 Correct contents in A: and B:
 MP8 Correct value in Answer:

Label	Contents
A:	86
B:	150
Answer:	112

7(a)(i)

1 mark for each shaded section

Instruction address	ACC	Memory address				
		10	11	12	13	14
		12	11	10	22	22
100	12					
101	22					
102			22			
103						
104						
107	22					

7(a)(ii)

1 mark from:

- The number 10 will be loaded into the ACC instead of 12 / contents of address 10
- The addition will give 20 not 22 so the comparison will fail and result in an infinite loop

7(a)(iii)

1 mark for name of mode, **1 mark** for matching description

e.g.

- Indirect
 - The operand points to the memory location that contains the address of the data
- Indexed
 - The address of the data is formed by adding the contents of the Index Register (IX) to the operand
- Relative
 - The address is calculated using its distance from a base address

7(b)(i)

1 mark for:

1111 1111

7(b)(ii)

1 mark for:

0000 0011

5(a)(i)	1 mark for each shaded section																																																																																								
	<table><tr><th rowspan="2">Instruction address</th><th rowspan="2">ACC</th><th colspan="4">Memory address</th></tr><tr><th>50</th><th>51</th><th>52</th><th>53</th></tr><tr><td></td><td></td><td>47</td><td>48</td><td>49</td><td>50</td></tr><tr><td>500</td><td>50</td><td></td><td></td><td></td><td></td></tr><tr><td>501</td><td>49</td><td></td><td></td><td></td><td></td></tr><tr><td>502</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>504</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>501</td><td>48</td><td></td><td></td><td></td><td></td></tr><tr><td>502</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>503</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>505</td><td></td><td>48</td><td></td><td></td><td></td></tr><tr><td>506</td><td>38</td><td></td><td></td><td></td><td></td></tr><tr><td>507</td><td></td><td></td><td>38</td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr></table>	Instruction address	ACC	Memory address				50	51	52	53			47	48	49	50	500	50					501	49					502						504						501	48					502						503						505		48				506	38					507			38														
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5(a)(ii)	1 mark for addressing mode, 1 mark for matching description • Direct • The operand is the address of the data • Indirect • The operand points to the memory location which is the address of the data • Indexed • The address of the data is formed by adding the contents of the Index Register (IX) to the operand																																																																																								
5(b)	1 mark for each correct instruction e.g. AND B00000000 / #0 / &0 OR B10000000 / #128 / &80																																																																																								

8(a)

1 mark for each correct content of the ACC (4)
1 mark for correct IX column

	Instructions	ACC content	IX content
1	LDM #19 DEC ACC	18	20
2	LDD 23 ADD 19	40	20
3	LDI 25 INC ACC	5	20
4	LDR #21 LDX 2	15	21

8(b)(i)

1 mark each correct content of ACC

	Instructions	ACC content
1	LSL #2	0110 1000
2	ADD #5 AND #30	0001 1110
3	OR B11110010 INC ACC	1111 1011

8(b)(ii)

1 mark each to max 2 for explanation

- An odd binary number will have a 1 in the Least Significant Bit (LSB)
- A bit manipulation operation is required to access/mask only the LSB and clear all the others
- Compare the result of the masking with denary 1
- ... the result of the comparison will be true if the number is odd

1 mark for correct instruction

- AND B00000001 // AND #1 // AND &01

4(a)

1 mark for each correct answer:

Program Number	Code	ACC Content
1	LDD 20 ADD #2	4
2	LDX 22	5
3	LDI 25 INC ACC SUB 22	1
4	LDD 19 LDM #5 LDM #25	25

4(b)

1 mark for each correct answer:

Program Number	Code	ACC Content
1	AND 31	1001 1010
2	XOR B01001111	1101 0101
3	OR #30	1001 1110