<table>
<tr><td>6(a)</td><td>1 mark for each correct description, max 2 marks

<table>
<tr><th>Register</th><th>Role</th></tr>
<tr><td>ACC</td><td>stores the intermediate results of arithmetic and logical operations
// holds the result of a calculation</td></tr>
<tr><td>CIR</td><td>holds the instruction currently being decoded and/or executed</td></tr>
</table>
</td></tr>
<tr><td>6(b)</td><td>1 mark per bullet point, max 2 marks

e.g.

• Latency may be increased
• … because the cores must communicate with one another

• There is a potential for dead-lock situations
• … where one core may wait for information from other cores which in turn are waiting for the first one

• Not all software is designed to use multi-cores
• ... so some of the additional cores would be idle

• Increased heat generation
• ... which could cause damage to other components</td></tr>
<tr><td>6(c)</td><td>1 mark per bullet point, max 3 marks

• DRAM requires to be refreshed/charged SRAM does not request a refresh
• DRAM stores each bit as charge SRAM uses flip-flop to store each bit
• DRAM is less expensive to manufacture SRAM is more expensive to manufacture
• DRAM has slower access speeds SRAM has faster access times
• DRAM has higher storage/bit/data density SRAM has lower storage/bit/data density
• DRAM is used in main memory SRAM is used in cache</td></tr>
</table>