

4.1.1 Registers, interrupts, ports and performance

Name: _____ Class: _____ Date: _____

Total: 40 marks

KEY WORDS register transfer notation 寄存器传送记法 • interrupt 中断
• interrupt service routine 中断服务程序 • port 端口 • address bus 地址总线

Objective

Build the skills to answer exam questions on the parts of **CPU architecture** that sheet 4.1 only touches: **register transfer notation** 寄存器传送记法 for the fetch-execute cycle, every special purpose register, the system clock and the **Immediate Access Store** 立即存取存储器, bus widths, **interrupts** 中断, **ports** 端口, and the factors that affect performance. This sheet covers syllabus 4.1.

You must be able to:

- explain the Von Neumann model for a computer system and the stored program concept
- state the role of each special purpose register, and the difference between general purpose and special purpose registers
- describe the roles of the Arithmetic and Logic Unit (ALU), the Control Unit (CU), the system clock and the Immediate Access Store (IAS)
- describe how the address bus, data bus and control bus transfer data, and work out the effect of a bus width
- describe the stages of the fetch-execute cycle in register transfer notation
- explain the causes and uses of interrupts, when they are detected, and how an Interrupt Service Routine (ISR) handles them
- explain how processor type, the number of cores, bus width, clock speed and cache memory affect performance
- choose a suitable port (USB, HDMI or VGA) for a peripheral device

1 Worked examples

Study these first. Each one shows a **method** that a question later on this sheet needs.

■ The stored program concept and the registers

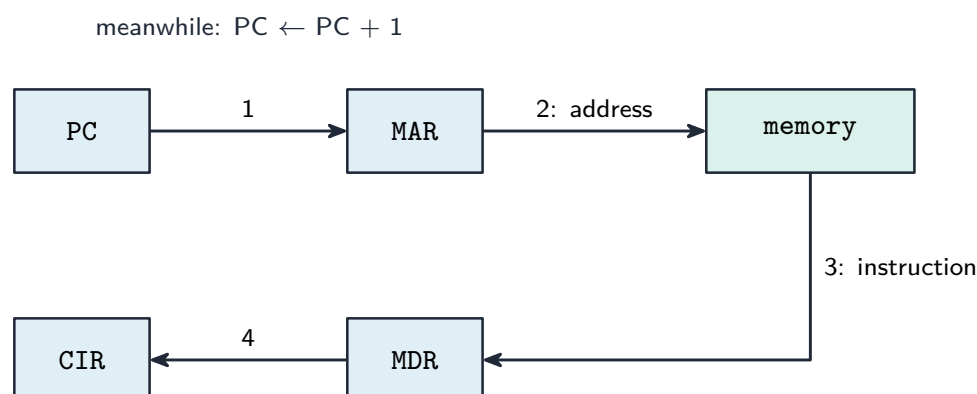
In the **Von Neumann** model, program instructions and data are stored together in the same memory, the **Immediate Access Store** (main memory). The processor fetches the instructions from memory one at a time and executes them in order: this is the **stored program concept**.

register	purpose
Program Counter (PC)	holds the address of the next instruction to be fetched
Memory Address Register (MAR)	holds the address of the memory location to be read or written
Memory Data Register (MDR)	holds the data or instruction just read from memory, or about to be written to it
Current Instruction Register (CIR)	holds the instruction being decoded and executed
Accumulator (ACC)	holds the value being worked on and the result of each ALU operation
Index Register (IX)	holds a value that is added to an address, to step through a list of memory locations
Status Register (SR)	holds flags, such as carry, negative, zero and overflow, set by the result of an operation

- A **special purpose register** has one fixed job in the fetch-execute cycle. A **general purpose register**, such as the ACC in many processors, holds whatever values a program is working on.
- The **system clock** sends timing signals that keep the components working in step. The **Control Unit** decodes each instruction and sends control signals, and the **ALU** carries out arithmetic and logic operations.

■ Register transfer notation

[PC] means the contents of the PC, and $\leftarrow$ means "is copied into". [[MAR]] means the contents of the memory location whose address is held in the MAR.



step	register transfer notation	in words
1	$\text{MAR} \leftarrow [\text{PC}]$	the address of the next instruction is copied from the PC to the MAR
2	$\text{PC} \leftarrow [\text{PC}] + 1$	the PC is increased by 1, so it points at the next instruction
3	$\text{MDR} \leftarrow [[\text{MAR}]]$	the instruction at that address is copied into the MDR
4	$\text{CIR} \leftarrow [\text{MDR}]$	the instruction is copied into the CIR, ready to be decoded

- Step 2 may also come after step 3: the PC only has to be increased before the next fetch.
- After the fetch, the Control Unit **decodes** the instruction in the CIR, and then it is **executed**.

■ Buses and bus width

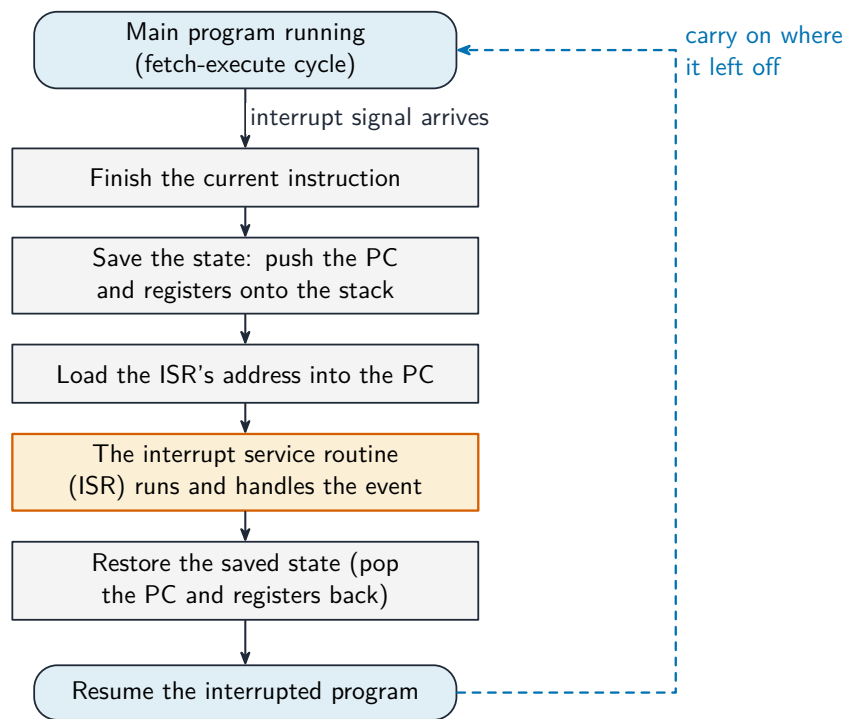
bus	carries	direction
address bus	memory addresses, from the processor to memory	one-way
data bus	data and instructions, between the processor, memory and devices	two-way
control bus	control signals, such as memory read, memory write, clock and interrupt signals	two-way

- An address bus with n lines can carry 2^n different addresses. A 16-bit address bus can address $2^{16} = 65\,536$ locations, and a 32-bit address bus can address 2^{32} locations, which is 4 GiB of bytes.
- A wider **data bus** moves more bits in each transfer, so more data moves per second.

■ Interrupts

An **interrupt** is a signal from hardware or software that tells the processor something needs attention.

- **Hardware** causes: a key is pressed, a printer runs out of paper, a timer signal.
- **Software** causes: division by zero, an attempt to use a memory location that is not allowed, a request for an operating system service.



1. The processor checks for interrupts at the **end of each fetch-execute cycle**, before the next instruction is fetched.
2. If the interrupt has a higher priority than the current task, the contents of the PC and the other registers are saved on the **stack 栈**.
3. The address of the **Interrupt Service Routine 中断服务程序 (ISR)** is loaded into the PC, and the ISR runs and deals with the event.
4. The saved contents are restored, and the interrupted program carries on where it stopped.

■ Performance and ports

factor	why it affects performance
processor type	a newer design does more work in each clock cycle
number of cores	each core fetches and executes instructions, so several tasks run at the same time
bus width	a wider data bus moves more bits per transfer; a wider address bus allows more memory
clock speed	more clock cycles per second means more instructions per second
cache memory	fast memory next to the processor means fewer slow fetches from main memory

- More cores only help when the software can divide its work between them.

port	carries	typical use
Universal Serial Bus (USB)	data both ways, and power; plug and play	keyboard, mouse, flash drive, external hard disk, printer
High Definition Multimedia Interface (HDMI)	high definition digital video and sound	monitor, television, projector
Video Graphics Array (VGA)	analogue video only, no sound	older monitors and projectors

2 Practice

Now use the methods above.

2.1 Explain what is meant by the **stored program concept**. [2]

2.2 Describe the step $MDR \leftarrow [[MAR]]$. [2]

2.3 State the purpose of the **Status Register** and of the **Index Register**. [2]

2.4 A processor has a 24-bit address bus. Calculate how many different memory locations it can address. [2]

2.5 Identify the most suitable port for each device.

(a) a keyboard [1]

(b) a television that must receive high definition video and sound [1]

(c) an old projector with an analogue video input [1]

2.6 Give **two** hardware causes and **one** software cause of an interrupt. [3]

3 Exam-style questions

3.1 Complete the register transfer notation for the fetch stage of the fetch-execute cycle. [3]

step	register transfer notation
1	MAR $\leftarrow$ [PC]
2	_____
3	_____
4	_____

3.2 A student is typing a report when the printer, which is printing another document, runs out of paper.

(a) State whether this causes a hardware interrupt or a software interrupt, and give a reason. [1]

(b) **Explain** how the processor detects and handles this interrupt. [5]

(c) **Explain** why the contents of the registers must be saved. [2]

3.3 Two computers are for sale.

	computer A	computer B
number of cores	4	8
clock speed	3.6 GHz	3.0 GHz
cache memory	8 MB	16 MB

A video-editing company wants the computer that will edit video faster. **Explain** how **each** of the three factors affects performance, and state which computer the company should choose. [5]

3.4 (a) State the number of different memory locations that can be addressed with a 20-bit address bus. [1]

(b) **Explain** the effect of doubling the width of the data bus. [2]

(c) Identify **two** signals carried on the control bus. [2]

3.5 A student connects a monitor, a keyboard and an external hard disk to a laptop.

(a) Identify a suitable port for each device. [3]

(b) The monitor also has a VGA input. **Explain** why the picture may be worse through the VGA port than through the HDMI port. [2]
