Past-paper walk-through

Central Processing Unit (CPU) Architecture ▪ 4.1

eXercise

Questions in this set

- 9618/11 N25 Q6 ▪ 7 marks
- 9618/12 J25 Q1 ▪ 9 marks
- 9618/13 J25 Q2 ▪ 10 marks
- 9618/11 N24 Q3 ▪ 16 marks
- 9618/11 N24 Q8 ▪ 4 marks
- 9618/12 N24 Q3 ▪ 12 marks

Reading the mark scheme

- **B1** a mark that stands on its own – the point is either made or not.
- **M1** a *method* mark: the right approach, even if the number is wrong.
- **A1** an *answer* mark, and it usually needs its M mark first.
- **C1** a working mark on the way to the answer.
- // separates answers the examiner accepts equally.
- **ecf** = error carried forward: a later part is marked on your own earlier answer.
- **owtte** = "or words to that effect" – the wording need not match.

Question 6

9618/11 N25 ▪ Q6 ▪ 7 marks

The processor uses several registers, including the Accumulator (ACC) and the Current Instruction Register (CIR).

(a) Complete the table by describing the role of each register.

Register	**Role**
ACC	
CIR	

Question 6

[2]

Question 6

Register	Role
ACC	....
CIR	....

[2]

Question 6

9618/11 N25 ▪ Q6 ▪ 7 marks

The processor uses several registers, including the Accumulator (ACC) and the Current Instruction Register (CIR).

(b) Increasing the number of cores in a processor can affect the performance of a computer.

Describe the drawbacks of increasing the number of cores in a processor. **[2]**

Question 6

9618/11 N25 ▪ Q6 ▪ 7 marks

The processor uses several registers, including the Accumulator (ACC) and the Current Instruction Register (CIR).

(c) State **three** differences between Dynamic RAM (DRAM) and Static RAM (SRAM).

1. 2. 3. **[3]**

Solution 6

(a)

Mark scheme

- 1 mark for each correct description, max 2 marks
- Register
- Role
- ACC stores the intermediate results of arithmetic and logical operations
- // holds the result of a calculation
- CIR holds the instruction currently being decoded and/or executed

Solution 6

(b) Mark scheme

- 1 mark per bullet point, max 2 marks e.g.
- ▪ Latency may be increased
- ▪ ... because the cores must communicate with one another
- ▪ There is a potential for dead-lock situations
- ▪ ... where one core may wait for information from other cores which in turn are waiting for the first one
- ▪ Not all software is designed to use multi-cores
- ▪ ... so some of the additional cores would be idle

Solution 6

- Increased heat generation
- ... which could cause damage to other components

Solution 6

(c) Mark scheme

- 1 mark per bullet point, max 3 marks
- ▪ DRAM requires to be refreshed/charged SRAM does not request a refresh
- ▪ DRAM stores each bit as charge SRAM uses flip-flop to store each bit
- ▪ DRAM is less expensive to manufacture SRAM is more expensive to manufacture
- ▪ DRAM has slower access speeds SRAM has faster access times
- ▪ DRAM has higher storage/bit/data density SRAM has lower storage/bit/data density

Solution 6

- ▪ DRAM is used in main memory SRAM is used in cache
- 3
- October/November
- 2025

Question 1

9618/12 J25 ▪ Q1 ▪ 9 marks

The table has six statements about the Von Neumann model for a computer system. Three of the statements are incorrect.

Statement number	Statement
1	The Program Counter (PC) stores the next instruction to be fetched from memory.
2	The Arithmetic and Logic Unit (ALU) performs mathematical and logical operations.
3	The Control Unit (CU) sends signals to other components on the data bus.
4	The Memory Data Register (MDR) transfers data to the memory address stored in the Memory Address Register (MAR).
5	The MAR stores an address from memory.
6	The Accumulator (ACC) stores the result of calculations.

Question 1

(a) Complete the table by writing the **three** incorrect statement numbers and the corrected statements.

Incorrect statement number	**Corrected statement**

[3]

Question 1

Incorrect statement number	Corrected statement
.....	.....
	.....
	.....
.....	.....
	.....
	.....
.....	.....
	.....
	.....

Question 1

	.....

[3]

Question 1

Statement number	Statement
1	The Program Counter (PC) stores the next instruction to be fetched from memory.
2	The Arithmetic and Logic Unit (ALU) performs mathematical and logical operations.
3	The Control Unit (CU) sends signals to other components on the data bus.
4	The Memory Data Register (MDR) transfers data to the memory address stored in the Memory Address Register (MAR).
5	The MAR stores an address from memory.
6	The Accumulator (ACC) stores the result of calculations.