Past-paper walk-through

Logic Gates and Logic Circuits ▪ 3.2

eXercise

Questions in this set

- 9618/11 N25 Q3 ▪ 4 marks
- 9618/13 N25 Q3 ▪ 4 marks
- 9618/32 N25 Q6 ▪ 9 marks
- 9618/11 J25 Q1 ▪ 4 marks
- 9618/32 J25 Q7 ▪ 8 marks
- 9618/33 J25 Q3 ▪ 8 marks
- 9618/11 N24 Q5 ▪ 6 marks
- 9618/13 N24 Q1 ▪ 5 marks
- 9618/12 J24 Q1 ▪ 6 marks

Reading the mark scheme

- **B1** a mark that stands on its own – the point is either made or not.
- **M1** a *method* mark: the right approach, even if the number is wrong.
- **A1** an *answer* mark, and it usually needs its M mark first.
- **C1** a working mark on the way to the answer.
- // separates answers the examiner accepts equally.
- **ecf** = error carried forward: a later part is marked on your own earlier answer.
- **owtte** = "or words to that effect" – the wording need not match.

Question 3

9618/11 N25 ▪ Q3 ▪ 4 marks

(a) Draw a logic circuit for the logic expression:

$$X = \text{NOT } ((A \text{ NAND } B) \text{ XOR } (\text{NOT } A \text{ OR NOT } C))$$

[2]

Question 3

R	S	T	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Question 3

9618/11 N25 ▪ Q3 ▪ 4 marks

(b) Write the logic expression for the following truth table.

R	S	T	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Question 3

[2]

Solution 3

(a) Worked steps

Build it from the inside out, exactly as the brackets are nested.

- **Innermost, left:** a NAND gate with inputs A and B.
- **Innermost, right:** NOT A and NOT C (two inverters), feeding an OR gate.
- **Middle:** an XOR gate taking those two results as its inputs.
- **Outermost:** an inverter on the XOR's output, giving X.

Solution 3

Each of the two marks covers one layer: the pair of bracketed sub-expressions, then the XOR with its final NOT. Draw the inverters as separate gates rather than as bubbles unless the paper's own symbol set uses bubbles — and label every input line, since an unlabelled circuit cannot be marked.

Mark scheme

- One mark per bullet point, max 2 marks
- ▪ (A NAND B) and (NOT A OR NOT C)
- ▪ XOR and NOT

Solution 3

(b)

Mark scheme

- 1 mark per bullet point, max 2 marks
- ▪ One correct term: (R AND S AND NOT T)
- // (NOT R AND NOT S AND T)
- ▪ Second correct term plus the OR in correct place
- Answer:
- Q = (R AND S AND NOT T) OR (NOT R AND NOT S AND T)

Question 3

9618/13 N25 ▪ Q3 ▪ 4 marks

(a) Complete the truth table for the following logic expression:

$$X = (A \text{ NOR } B) \text{ NAND } (C \text{ XOR } B)$$

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Question 3

[2]

Question 3

A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Question 3

9618/13 N25 ▪ Q3 ▪ 4 marks

(b) Draw a logic circuit for the logic expression:

$$X = \text{NOT } (((A \text{ AND } B) \text{ OR } C) \text{ AND } (C \text{ NOR } D))$$

[2]

Solution 3

(a) Worked steps

Work the circuit **gate by gate**, and give each intermediate signal its own column. Do not try to see the whole answer at once.

- Add a column for the output of every gate, in the order the signals flow: the first-level gates, then whatever they feed.
- Fill each row left to right. Each column depends only on columns already filled, so there is never anything to guess.
- Only the last column is the circuit's output X.

Solution 3

Two marks, one per shaded region of the table, so the intermediate columns are where the reliability comes from — a row worked in your head is a row you cannot check. The inputs go in **counting order**: 000, 001, 010, 011, 100, 101, 110, 111. Three inputs give $2^3 = 8$ rows; a table with fewer rows has a missing combination. **Mark scheme**

- 1 mark per shaded area, max 2 marks
- A
- B
- C
- X

Solution 3

- 0
- 0
- 0
- 1
- 0
- 0
- 1
- 0
- 0
- 1

Solution 3

- 0
- 1
- 0
- 1
- 1
- 1
- 1
- 0
- 0
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Solution 3

- 1
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- 1
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- 1
- 0
- 1
- 1
- 1

Solution 3

- 1
- 1

Solution 3

(b) Worked steps

Write the expression the same way you filled the table: **outwards from the inputs**, naming each gate's output as you go.

- The first branch combines A and B with AND, and that result with C using OR: `A AND B OR C`.
- The second branch is C NOR D.
- The final gate combines those two, and the operator it uses is the last thing in the expression.

Two marks: one for `A AND B OR C`, one for the `C NOR D` part together with the final two gates.

Solution 3

Bracket the sub-expressions even where precedence would allow you not to. `A AND B OR C` and `A AND (B OR C)` are different circuits, and a bracket costs nothing while an ambiguity costs a mark.

Mark scheme

- 1 mark per bullet point, max 2 marks
- ▪ A AND B OR C
- ▪ C NOR D and final two gates

Question 6

9618/32 N25 ▪ Q6 ▪ 9 marks

The diagram shows a logic circuit.

(a) Complete the truth table for the given logic circuit. Show your working.

			Working space				
A	**B**	**C**	**P**	**Q**	**R**	**S**	**Z**
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

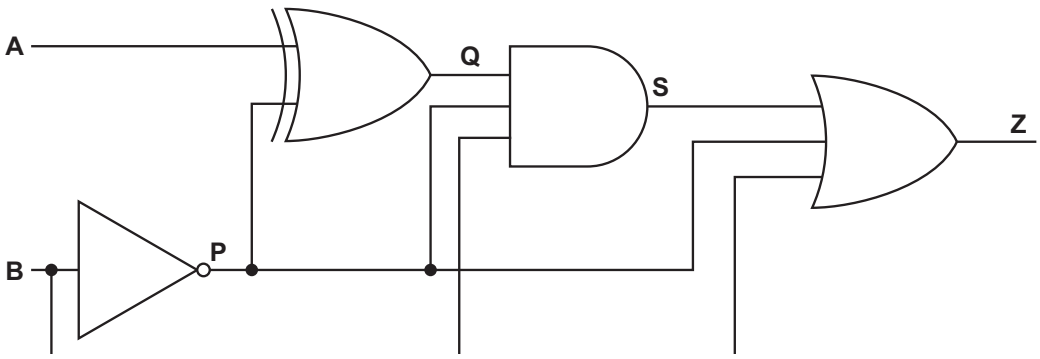
Question 6

[3]

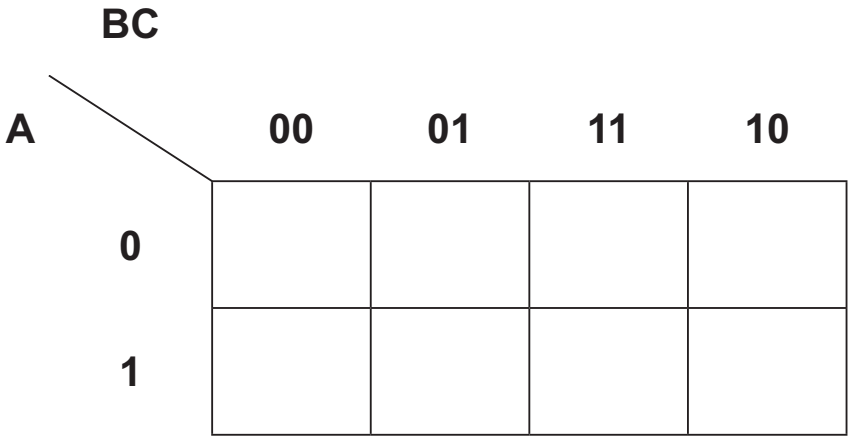
Question 6

			Working space				
A	**B**	**C**	**P**	**Q**	**R**	**S**	**Z**
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

Question 6



Question 6



Question 6

9618/32 N25 ▪ Q6 ▪ 9 marks

The diagram shows a logic circuit.

(b)(i) Complete the Karnaugh map (K-map) for the Boolean expression:

$$\mathbf{A.B.C} + \mathbf{A.B.C} + \mathbf{A.B.C} + \mathbf{A.B.C}$$

A \ BC	**00**	**01**	**11**	**10**
0				
1				

Question 6

[2]

(b)(ii) Draw loop(s) around appropriate group(s) in the K-map to produce an optimal sum-of-products. **[2]**

(b)(iii) Write the Boolean expression from your answer to part **b(ii)** as a simplified sum-of-products. Do **not** carry out any further simplification. **[2]**

Solution 6

(a) Worked steps

The working columns are worth a mark on their own, so fill them in rather than jumping to Z.

- Give every intermediate signal its own column: P, Q, R, S, then Z.
- Work **gate by gate, left to right**: each column depends only on columns already filled.
- Do all eight rows of one column before starting the next. Going row by row across the whole circuit is where mistakes creep in, and one wrong intermediate value corrupts every Z beneath it.
- Read each gate carefully: an inverting output (NAND, NOR) is the opposite of the gate it looks like, and a small circle on the symbol is the only thing telling you so.

Solution 6

Mark scheme

- ▪ One mark for working, (all four columns P, Q, R and S)
- ▪ One mark for first four rows of column Z
- ▪ One mark for second four rows of column Z
- Working space
- A
- B
- C
- P

Solution 6

- Q
- R
- S
- Z
- 0
- 0
- 0
- 1
- 1
- 0

Solution 6

- 0
- 1
- 0
- 0
- 1
- 1
- 1
- 1
- 1
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Solution 6

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Solution 6

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Solution 6

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Solution 6

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Solution 6

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- 1
- 0
- 1
- 0
- 0
- 0

Solution 6

(b)(i) Mark scheme

- Two marks if no errors present
- One mark if only one error present
- BC
- A
- 00
- 01
- 11
- 10

Solution 6

- 0
- 0
- 1
- 1
- 0
- 1
- 0
- 1
- 0
- 1

Solution 6

- 2
- October/November
- 2025

Solution 6

(b)(ii) Worked steps

- Loop only 1s, in groups of 1, 2, 4 or 8 — never 3 or 6.
- Make each loop as large as it can be, and let loops overlap where that allows a bigger one.
- Remember the map wraps left-to-right and top-to-bottom.
- Use the fewest loops that cover every 1; each loop is one term of the sum-of-products, made of the variables that stay constant across it.

Mark scheme

- One mark for each correct loop (Max 2)

Solution 6

- BC
- A
- 00
- 01
- 11
- 10
- 0
- 0
- 1
- 1

Solution 6

- 0
- 1
- 0
- 1
- 0
- 1

Solution 6

(b)(iii) Mark scheme

- One mark for each mark point (Max 2)
- ▪ One correct Boolean term with a + / OR sign
- ▪ All Boolean terms and operators correct and no other terms present
- _ _ _
- A.C + B.C + A.B.C
- 2
- October/November
- 2025

Question 1

9618/11 J25 ▪ Q1 ▪ 4 marks

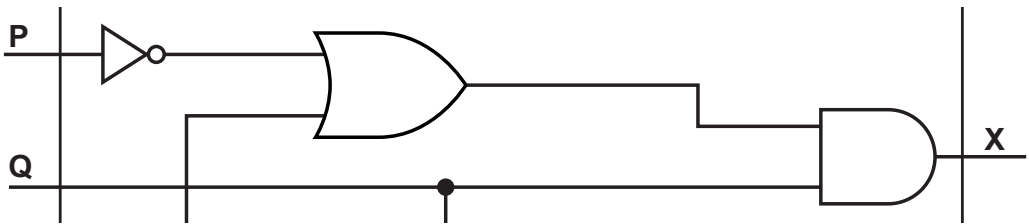
(a) Write the logic expressions for the following logic circuit. **[2]**

Question 1

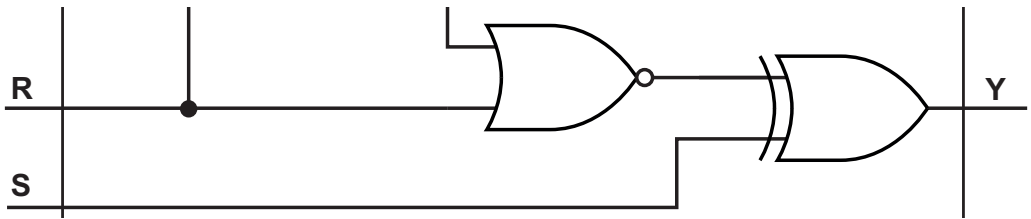
A	B	C	Working space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[2]

Question 1



Question 1



Question 1

9618/11 J25 ▪ Q1 ▪ 4 marks

(b) Complete the truth table for the following logic circuit.

A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Question 1

[2]

Solution 1

(a)

Mark scheme

- 1 mark each:
- X = Q AND (NOT P OR R)
- Y = S XOR (Q NOR R)

Solution 1

(b) Mark scheme

- 1 mark for first 4 rows, 1 mark for second 4 rows
- A
- B
- C
- Working space
- X
- 0
- 0

Solution 1

- 0
- 1
- 0
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Solution 1

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Solution 1

- 1
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Question 7

9618/32 J25 ▪ Q7 ▪ 8 marks

The diagram shows a logic circuit.

(a) Complete the truth table for the given logic circuit. Show your working.

				Working space				
A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**	**Z**
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Question 7

[3]

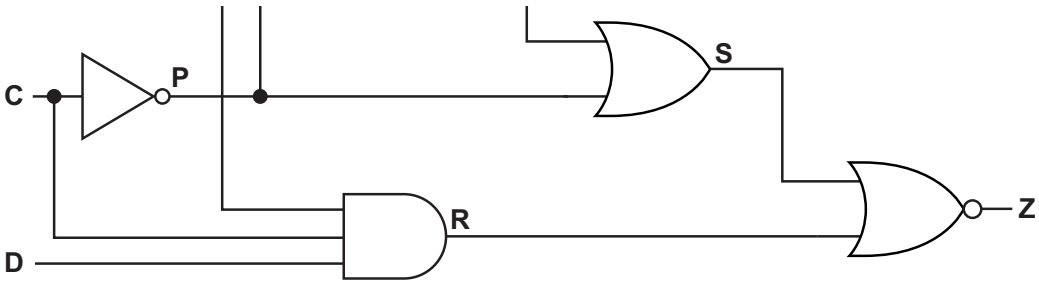
Question 7

				Working space				
A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**	**Z**
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					

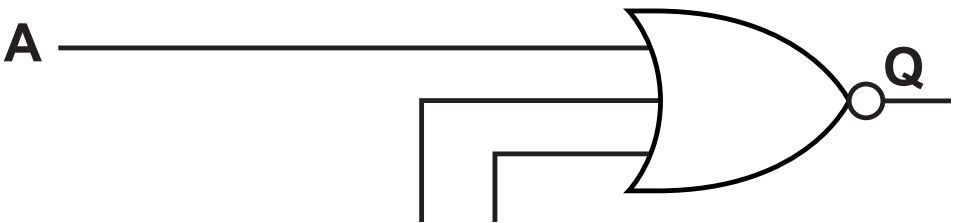
Question 7

1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					

Question 7



Question 7



Question 7

9618/32 J25 ▪ Q7 ▪ 8 marks

The diagram shows a logic circuit.

(b) Write the Boolean logic expression that corresponds to the given logic circuit as the sum-of-products. **[1]**

Question 7

9618/32 J25 ▪ Q7 ▪ 8 marks

The diagram shows a logic circuit.

(c) Use Boolean algebra including De Morgan's laws to simplify the following expression. Show all working.

$$(\overline{A + B}) \cdot (\overline{A \cdot B + B \cdot C})$$

[4]

Solution 7

(a) Worked steps

Four inputs mean **16 rows**, and the working space provides a column for each internal signal — P, Q, R and S — precisely so you do not have to hold the circuit in your head.

- Fill P, Q, R and S first, gate by gate, for all 16 rows.
- Then fill Z from whichever of those the final gate takes.

Three marks: one for the four working columns, one for the first eight rows of Z, one for the second eight. So the working columns are not optional — they carry a mark of their own, and they are what makes the two halves of Z consistent.

Write the inputs in counting order, 0000 to 1111. A quick check on the pattern: column D alternates every row, C every two, B every four, A every eight. If your table does not look like that, a combination is missing or repeated. **Mark scheme**

Solution 7

- One mark for working, (all four columns P, Q, R and S)
- One mark for first eight rows of column Z (Shaded)
- One mark for second eight rows of column Z (Unshaded)
- Working space
- A
- B
- C
- D

Solution 7

- P
- Q
- R
- S
- Z
- 0
- 0
- 0
- 0
- 1

Solution 7

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Solution 7

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Solution 7

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Solution 7

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Solution 7

(b)

Mark scheme

- One mark for correct answer (terms may be in any order)
- $Z = A.B.C.D + A.B.C.D + A.B.C.D + A.B.C.D$

Solution 7

(c) Worked steps

Four marks, and the mark scheme awards them for **naming and applying the right law at each step**, so set the simplification out one law per line.
Starting from $(\overline{A + B}) \cdot (A \cdot B + B \cdot C)$:

- **De Morgan's laws** turn the complement of a sum into a product of complements: $\overline{A + B} = \overline{A} \cdot \overline{B}$.
- **Distributive law** multiplies the bracket out.
- **Idempotent laws** collapse repeats: $A \cdot A = A$ and $A + A = A$.
- **Absorption** removes a term already implied by another: $A + A \cdot B = A$.

Solution 7

Two habits earn the marks. **Name the law beside each line** — the marks are for correct application of De Morgan's, then two more for idempotent, distributive or absorption, so an unlabelled chain of algebra makes the examiner guess. And **change one thing per line**; combining three steps into one is where sign and bracket errors enter, and it makes a partly correct answer unmarkable.
De Morgan's is the step to do first whenever a complement sits over a whole bracket, because nothing else can be applied until it is broken up. **Mark scheme**

- One mark for each mark point
- ▪ Correct application of De Morgan's laws
- ▪ Correct application of Idempotent, Distributive or Absorption laws

Solution 7

- ▪ Correct application of Idempotent, Distributive or Absorption laws
- ▪ Correct final answer
- (A+B).(A.B+B.C)
- (A.B).(A+B+B+C)
- DeMorgan's laws
- (A.B).(A+B+C)
- Idempotent laws
- (A.A+A.B+A.C).(B.A+B.B+B.C)
- Distributive laws
- (A+A.B+A.C).(A.B+B+B.C)

Solution 7

- Idempotent laws
- (A+A.C).(B+B.C)
- Absorption laws
- A.B // A + B
- Absorption laws / Final Answer

Question 3

9618/33 J25 ▪ Q3 ▪ 8 marks

This truth table represents a logic circuit.

INPUT				OUTPUT
A	**B**	**C**	**D**	**Z**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Question 3

(a) Write the Boolean logic expression that corresponds to the given truth table as the sum-of-products. **[2]**

Question 3

INPUT				OUTPUT
A	**B**	**C**	**D**	**Z**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1

Question 3

1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Question 3