

4.1.1 Registers, interrupts, ports and performance

Name: _____ Class: _____ Date: _____ Total: 40 marks

KEY WORDS register transfer notation • interrupt
• interrupt service routine • port • address bus

Objective

Explain stored-program architecture; register roles and transfers; buses; interrupt handling; performance factors; USB, HDMI and VGA. Syllabus 4.1.

1 Key knowledge and worked examples

Study these first. Each one shows a **method** that a question later on this sheet needs.

■ The stored program concept and the registers

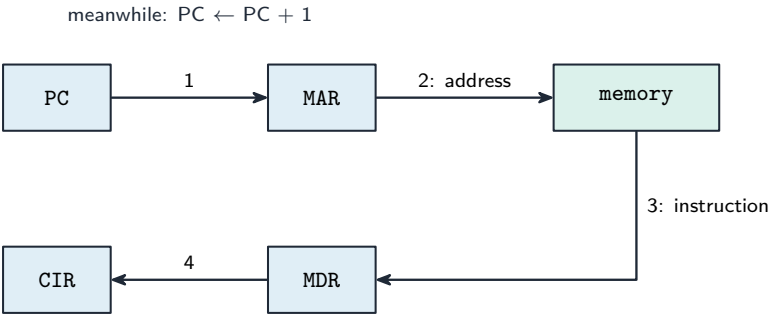
Stored program: data and instructions share main memory (IAS) in the Von Neumann model. The processor fetches, decodes and executes stored instructions.

register	purpose
Program Counter (PC)	address of the next instruction
Memory Address Register (MAR)	address of the current read/write location
Memory Data Register (MDR)	data/instruction being transferred to/from memory
Current Instruction Register (CIR)	instruction being decoded/executed
Accumulator (ACC)	ALU operands and results
Index Register (IX)	offset added to an address
Status Register (SR)	carry, negative, zero and overflow flags

- A **special purpose register** has one fixed job in the fetch-execute cycle. A **general purpose register**, such as the ACC in many processors, holds whatever values a program is working on.
- The **clock** synchronises components; the **Control Unit** decodes instructions and sends control signals; the **ALU** performs arithmetic and logic.

■ Register transfer notation

[PC] means the contents of the PC, and $\leftarrow$ means "is copied into". $[[\text{MAR}]]$ means the contents of the memory location whose address is held in the MAR.



step	register transfer notation	in words
1	$\text{MAR} \leftarrow [\text{PC}]$	the address of the next instruction is copied from the PC to the MAR
2	$\text{PC} \leftarrow [\text{PC}] + 1$	the PC is increased by 1, so it points at the next instruction
3	$\text{MDR} \leftarrow [[\text{MAR}]]$	the instruction at that address is copied into the MDR
4	$\text{CIR} \leftarrow [\text{MDR}]$	the instruction is copied into the CIR, ready to be decoded

- Step 2 may also come after step 3: the PC only has to be increased before the next fetch.
- After the fetch, the Control Unit **decodes** the instruction in the CIR, and then it is **executed**.

■ Buses and bus width

bus	carries	direction
address bus	memory addresses, from the processor to memory	one-way
data bus	data and instructions, between the processor, memory and devices	two-way
control bus	control signals, such as memory read, memory write, clock and interrupt signals	two-way

- An address bus with n lines can carry 2^n different addresses. A 16-bit address bus can address $2^{16} = 65\,536$ locations, and a 32-bit address bus can address 2^{32}

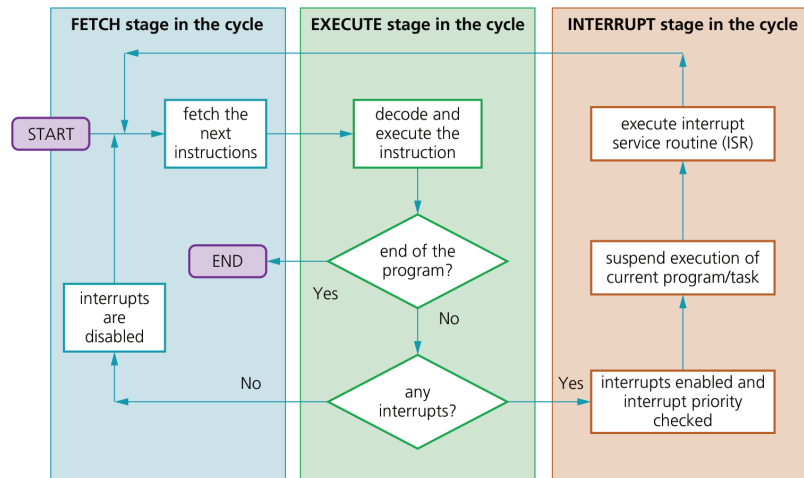
locations, addressing 4 GiB when each address selects one byte.

- A wider **data bus** transfers more bits at once, increasing throughput.

■ Interrupts

An **interrupt** is a signal from hardware or software that tells the processor something needs attention.

- **Hardware** causes: a key is pressed, a printer runs out of paper, a timer signal.
- **Software** causes: division by zero, an attempt to use a memory location that is not allowed, a request for an operating system service.



1. The processor checks for interrupts at the **end of each fetch-execute cycle**, before the next instruction is fetched.
2. If the interrupt has a higher priority than the current task, the contents of the PC and the other registers are saved on the **stack**.
3. The address of the **Interrupt Service Routine** (ISR) is loaded into the PC, and the ISR runs and deals with the event.
4. Restore the saved registers and resume the interrupted program.

■ Performance and ports

factor	why it affects performance
processor type	architecture affects work per clock cycle
number of cores	each core fetches and executes instructions, so several tasks run at the same time
bus width	a wider data bus moves more bits per transfer; a wider address bus allows more memory
clock speed	higher frequency can increase instruction rate; cycles per instruction vary
cache memory	fast memory next to the processor means fewer slow fetches from main memory

- More cores only help when the software can divide its work between them.

port	carries	typical use
USB	data both ways, and power; plug and play	keyboard, storage, printer
HDMI	high definition digital video and sound	monitor, television, projector
VGA	analogue video only, no sound	older monitors and projectors

2 Practice

Now use the methods above.

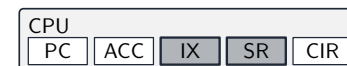
2.1 Explain what is meant by the **stored program concept**. [2]



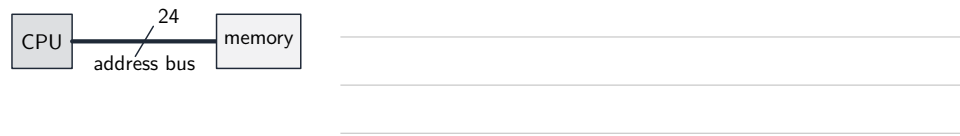
2.2 Describe the step $MDR \leftarrow [MAR]$. [2]



2.3 State the purpose of the **Status Register** and of the **Index Register**. [2]

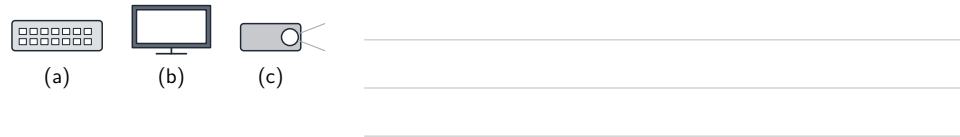


2.4 A processor has a 24-bit address bus. Calculate how many different memory locations it can address. [2]



2.5 Identify the most suitable port for each device. [1]

(a) a keyboard [1]



(b) a television that must receive high definition video and sound [1]

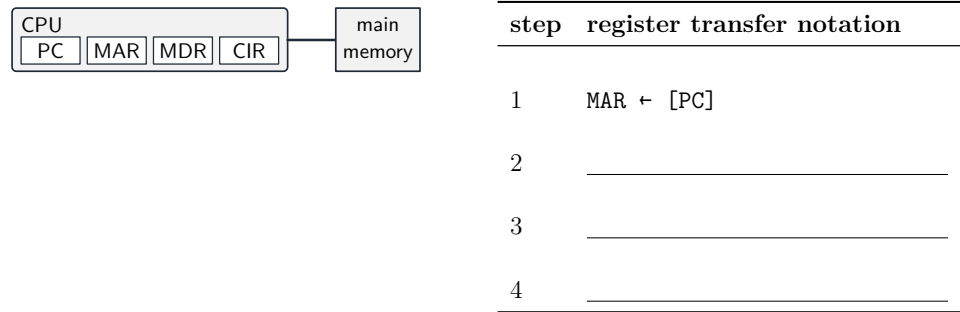
(c) an old projector with an analogue video input [1]

2.6 Give **two** hardware causes and **one** software cause of an interrupt. [3]



3 Exam-style questions

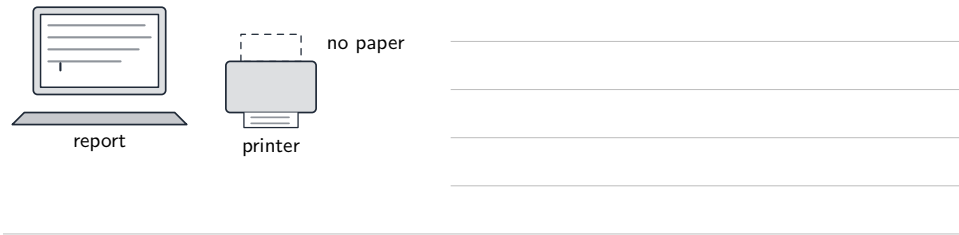
3.1 Complete the register transfer notation for the fetch stage of the fetch-execute cycle.[3]



3.2 A student is typing a report when the printer, which is printing another document, runs out of paper.

(a) State whether this causes a hardware interrupt or a software interrupt, and give a reason. [1]

(b) **Explain** how the processor detects and handles this interrupt. [5]



(c) **Explain** why the contents of the registers must be saved. [2]

3.3 Two computers are for sale.

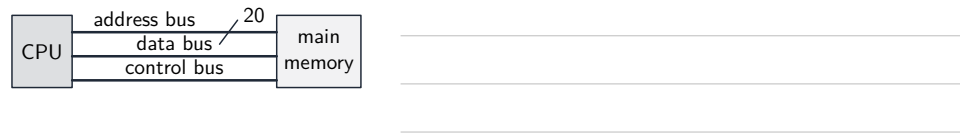
	computer A	computer B
number of cores	4	8
clock speed	3.6 GHz	3.0 GHz
cache memory	8 MB	16 MB

A video-editing company wants the computer that will edit video faster. **Explain** how **each** of the three factors affects performance, and state which computer the company should choose. [5]



3.4 (a) State the number of different memory locations that can be addressed with a 20-bit address bus. [1]

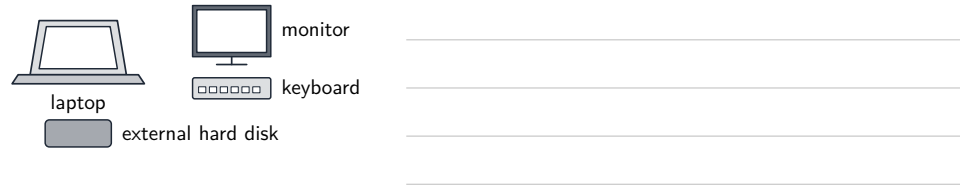
(b) **Explain** the effect of doubling the width of the data bus. [2]



(c) Identify **two** signals carried on the control bus. [2]

3.5 A student connects a monitor, a keyboard and an external hard disk to a laptop.

(a) Identify a suitable port for each device. [3]



(b) The monitor also has a VGA input. **Explain** why the picture may be worse through the VGA port than through the HDMI port. [2]